SONY

Diagonal 7.05 mm (Type 1/2.55) 12Mega-Pixel CMOS Image Sensor with Square Pixel for Color Cameras

# IMX363-AAQH5-C

## General description and application

IMX363-AAQH5-C is a diagonal 7.05mm (Type 1/2.55) 12 Mega-pixel CMOS active pixel type stacked image sensor with square pixel array. It adopts Exmor RS™ technology to achieve high speed image capturing by column parallel A/D converter circuits and high sensitivity and low noise image (comparing with conventional CMOS image sensor) through the backside illuminated imaging pixel structure. R, G, and B pigment primary color mosaic filter is employed. Each pixel is divided into right and left sub-pixel that can be driven independently or simultaneously. By introducing spatially multiplexed exposure technology, high dynamic range still pictures and movies are achievable. It equips an electronic shutter with variable integration time. It operates with four power supply voltages: analog 2.8 V and 1.8V, digital 1.05 V and 1.8 V for input/output interface and achieves low power consumption.
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## Functions and Features

- ◆ Back-illuminated and stacked CMOS image sensor Exmor RS
- ◆ Single Frame High Dynamic Range (HDR) with equivalent full pixels.
- ◆ High signal to noise ratio (SNR).
- ◆ Various output frame rate from Full resolution @30fps to WVGA @480fps
- ◆ Output video format of RAW10.
- ◆ Pixel binning readout and V sub-sampling function.
- ◆ Independent flipping and mirroring.
- ◆ CSI-2 serial data output (MIPI 2lane/4lane selectable, Max. 2.15Gbps/lane)
- ◆ 2-wire serial communication (Supports I2C "Fast-mode" and "Fast-mode Plus").
- ◆ Two PLLs for independent clock generation for pixel control and data output interface.
- ◆ Dynamic Defect Pixel Correction.
- ◆ Zero shutter lag.
- ◆ 29K bit of OTP ROM for users.
- ◆ Dual PD(Photo Diode)
- ◆ Phase difference pixel data output for Phase Detection Auto Focus(PDAF)

Exmor RS

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## Device Structure

- ◆CMOS image sensor
- ◆Image size : Diagonal 7.05 mm (Type 1/2.55)
- ◆Total number of pixels : 4048 (H) × 3168 (V) approx. 12.82 M pixels
- ◆Number of effective pixels : 4048 (H) × 3056 (V) approx. 12.37 M pixels
- ◆Number of active pixels : 4032 (H) × 3024 (V) approx. 12.19 M pixels
- ◆Chip size : 6.793 mm (H) × 5.668 mm (V)
- ◆Unit cell size : 1.4 µm (H) × 1.4 µm (V)
- ◆Sub-Pixel size : 0.7 µm (H) × 1.4 µm (V)
- ◆Substrate material : Silicon

## Absolute Maximum Ratings

| Item | Symbol | Ratings *Note | Unit | notes |
|---|---|---|---|---|
| Supply voltage (analog) | VANA1 | -0.3 to +3.3 | V | refer to Vss level |
| Supply voltage (analog) | VANA2 | -0.3 to +3.3 | V | |
| Supply voltage (digital) | VDIG | -0.3 to +1.8 | V | |
| Supply voltage (interface) | VIF | -0.3 to +3.3 | V | |
| Input voltage (digital) | VI | -0.3 to +3.3 | V | |
| Output voltage (digital) | VO | -0.3 to +3.3 | V | |
| Guaranteed Operating temperature | TOPR | -20 to +60 | ˚C | |
| Guaranteed storage temperature | TSTG | -30 to +80 | ˚C | |
| Guaranteed performance temperature | TSPEC | -20 to +60 | ˚C | |

## Recommended Operating Voltage

| Item | Symbol | Ratings | Unit | notes |
|---|---|---|---|---|
| Supply voltage (analog) | VANA1 | 2.8 ± 0.1 V | V | refer to Vss level |
| | VANA2* | 2.8V± 0.1 V<br>or<br>1.8 ± 0.1 V | V | |
| Supply voltage (digital) | VDIG | 1.05 ±0.1 | V | |
| Supply voltage (interface) | VIF | 1.8 ± 0.1 | V | |

Note: 1.8V operation is available. For details, please refer DC characteristics



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## Chip Center and Optical Center

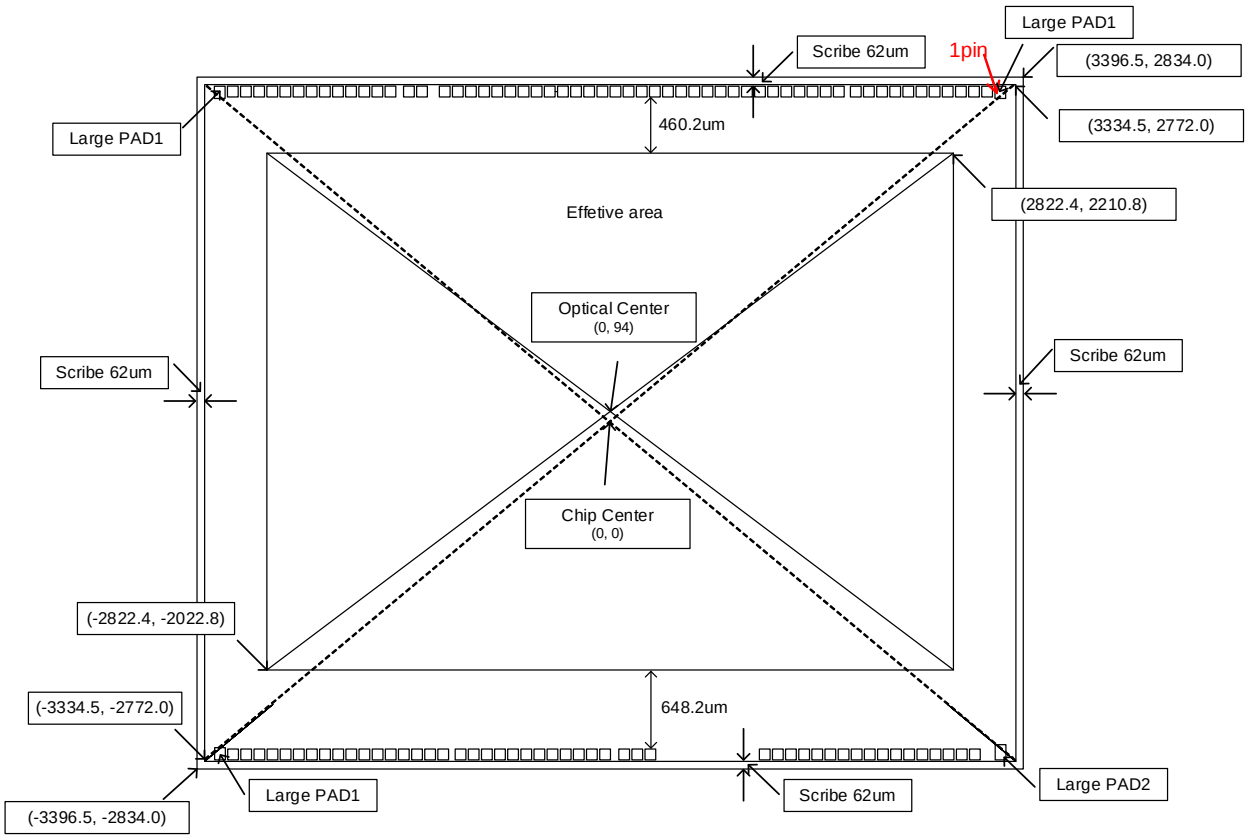


**Figure 1 Chip Center and Optical Center (x and y coordinates in µm)**



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## Pin Coordinates

**Table 1 Pin Coordinates**

| No. | Symbol | X | Y |
|---|---|---|---|
| 1 | VDDHPX1 | 3206.70 | 2709.25 |
| 2 | VSSHPX1 | 3098.70 | 2715.25 |
| 3 | VPI1 | 2990.70 | 2715.25 |
| 4 | VPISD1 | 2882.70 | 2715.25 |
| 5 | VRL1 | 2774.70 | 2715.25 |
| 6 | VRLRD1 | 2666.70 | 2715.25 |
| 7 | VDDHCP | 2558.70 | 2715.25 |
| 8 | VSSHCP | 2450.70 | 2715.25 |
| 9 | VDDHAN | 2342.70 | 2715.25 |
| 10 | VSSHAN | 2234.70 | 2715.25 |
| 11 | VDDHDA | 2126.70 | 2715.25 |
| 12 | VDDMDA | 2018.70 | 2715.25 |
| 13 | VDDMIO1 | 1879.20 | 2715.25 |
| 14 | XVS | 1771.20 | 2715.25 |
| 15 | SDA | 1663.20 | 2715.25 |
| 16 | SCL | 1555.20 | 2715.25 |
| 17 | INCK | 1447.20 | 2715.25 |
| 18 | VDDHFIL | 1339.20 | 2715.25 |
| 19 | VDDLSC1 | 1231.20 | 2715.25 |
| 20 | VSSLSC1 | 1123.20 | 2715.25 |
| 21 | VDDLSC2 | 1015.20 | 2715.25 |
| 22 | VSSLSC2 | 907.20 | 2715.25 |
| 23 | VDDLSC3 | 799.20 | 2715.25 |
| 24 | VSSLSC3 | 691.20 | 2715.25 |
| 25 | VDDLSC4 | 583.20 | 2715.25 |
| 26 | VSSLSC4 | 475.20 | 2715.25 |
| 27 | VDDMMD | 367.20 | 2715.25 |
| 28 | D4N | 259.20 | 2715.25 |
| 29 | D4P | 151.20 | 2715.25 |
| 30 | D2N | 43.20 | 2715.25 |
| 31 | D2P | -64.80 | 2715.25 |
| 32 | VSSLSC5 | -172.80 | 2715.25 |
| 33 | VDDLIF1 | -280.80 | 2715.25 |
| 34 | CKN | -388.80 | 2715.25 |
| 35 | CKP | -496.80 | 2715.25 |
| 36 | VDDLIF2 | -604.80 | 2715.25 |
| 37 | VSSLSC6 | -712.80 | 2715.25 |
| 38 | D1N | -820.80 | 2715.25 |
| 39 | D1P | -928.80 | 2715.25 |
| 40 | D3N | -1036.80 | 2715.25 |
| 41 | D3P | -1144.80 | 2715.25 |
| 42 | VSSLSC7 | -1252.80 | 2715.25 |
| 43 | VDDLSC7 | -1360.80 | 2715.25 |
| 44 | VDDLPL1 | -1547.10 | 2715.25 |
| 45 | VSSLPL1 | -1655.10 | 2715.25 |
| 46 | VDDLPL2 | -1806.30 | 2715.25 |
| 47 | VSSLPL2 | -1914.30 | 2715.25 |
| 48 | VDDLSC8 | -2022.30 | 2715.25 |
| 49 | VSSLSC8 | -2130.30 | 2715.25 |
| 50 | VDDLSC9 | -2238.30 | 2715.25 |

| No. | Symbol | X | Y |
|---|---|---|---|
| 51 | VSSLSC9 | -2346.30 | 2715.25 |
| 52 | VDDLSC10 | -2454.30 | 2715.25 |
| 53 | VSSLSC10 | -2562.30 | 2715.25 |
| 54 | VRLRD2 | -2670.30 | 2715.25 |
| 55 | VRL2 | -2778.30 | 2715.25 |
| 56 | VPISD2 | -2886.30 | 2715.25 |
| 57 | VPI2 | -2994.30 | 2715.25 |
| 58 | VSSHPX2 | -3102.30 | 2715.25 |
| 59 | VDDHPX2 | -3210.30 | 2709.25 |
| 60 | VDDLSC11 | -3208.50 | -2709.25 |
| 61 | VSSLSC11 | -3100.50 | -2715.25 |
| 62 | VDDLCN1 | -2992.50 | -2715.25 |
| 63 | VSSLCN1 | -2884.50 | -2715.25 |
| 64 | VDDLCN2 | -2776.50 | -2715.25 |
| 65 | VSSLCN2 | -2668.50 | -2715.25 |
| 66 | VSSLCN3 | -2560.50 | -2715.25 |
| 67 | VDDMCM1 | -2452.50 | -2715.25 |
| 68 | VDDHCM1 | -2344.50 | -2715.25 |
| 69 | VSSHPX3 | -2236.50 | -2715.25 |
| 70 | VDDHPX4 | -2128.50 | -2715.25 |
| 71 | VSSHPX4 | -2020.50 | -2715.25 |
| 72 | VRL3 | -1912.50 | -2715.25 |
| 73 | VRLRD3 | -1804.50 | -2715.25 |
| 74 | VDDSUB | -1696.50 | -2715.25 |
| 75 | VDDHPX5 | -1588.50 | -2715.25 |
| 76 | VSSHPX5 | -1480.50 | -2715.25 |
| 77 | VSSSUB | -1372.50 | -2715.25 |
| 78 | FSTROBE | -1230.30 | -2715.25 |
| 79 | SLASEL | -1122.30 | -2715.25 |
| 80 | GPO | -1014.30 | -2715.25 |
| 81 | SWDIO | -906.30 | -2715.25 |
| 82 | SWTCK | -798.30 | -2715.25 |
| 83 | TENABLE | -690.30 | -2715.25 |
| 84 | VDDLSC12 | -582.30 | -2715.25 |
| 85 | VSSLSC12 | -474.30 | -2715.25 |
| 86 | TEST1 | -366.30 | -2715.25 |
| 87 | TEST2 | -258.30 | -2715.25 |
| 88 | TEST3 | -150.30 | -2715.25 |
| 89 | TESTOUT | -42.30 | -2715.25 |
| 90 | POREN | 114.30 | -2715.25 |
| 91 | XCLR | 222.30 | -2715.25 |
| 92 | VDDMIO2 | 330.30 | -2715.25 |
| 93 | VSSHPX6 | 1269.90 | -2715.25 |
| 94 | VDDHPX6 | 1377.90 | -2715.25 |
| 95 | TVMON | 1485.90 | -2715.25 |
| 96 | TVCDSIN | 1593.90 | -2715.25 |
| 97 | VRLRD4 | 1701.90 | -2715.25 |
| 98 | VRL4 | 1809.90 | -2715.25 |
| 99 | VSSHPX7 | 1917.90 | -2715.25 |
| 100 | VDDHPX7 | 2025.90 | -2715.25 |



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| No. | Symbol | X | Y |
|---|---|---|---|
| 101 | VSSHPX8 | 2133.90 | -2715.25 |
| 102 | VDDHCM2 | 2241.90 | -2715.25 |
| 103 | VDDMCM2 | 2349.90 | -2715.25 |
| 104 | VSSLCN4 | 2457.90 | -2715.25 |
| 105 | VSSLCN5 | 2565.90 | -2715.25 |

| No. | Symbol | X | Y |
|---|---|---|---|
| 106 | VDDLCN5 | 2673.90 | -2715.25 |
| 107 | VSSLCN6 | 2781.90 | -2715.25 |
| 108 | VDDLCN6 | 2889.90 | -2715.25 |
| 109 | VSSLSC13 | 2997.90 | -2715.25 |
| 110 | VDDLSC13 | 3209.40 | -2697.00 |



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## Pin Description

**Table 2 Pin Description (Analog 2.8V and 1.8V operation)**

| No. | Symbol | I/O | A/D | Description | Remarks |
|---|---|---|---|---|---|
| 1 | VDDHPX1 | Power | A | 2.8V Power Supply | |
| 2 | VSSHPX1 | GND | A | 2.8V GND | |
| 3 | VPI1 | Power | A | 2.8V Input | Connect to VPI2 |
| 4 | VPISD1 | Power | A | 2.8V Input | Connect to VPISD2 |
| 5 | VRL1 | Minus | A | -1.2V Input | Connect to VRL2 ,VRL3 and VRL4 |
| 6 | VRLRD1 | Minus | A | -1.2V Input | Connect to VRLRD2 ,VRLRD3 and VRLRD4 |
| 7 | VDDHCP | Power | A | 2.8V Power Supply | |
| 8 | VSSHCP | GND | A | 2.8V GND | |
| 9 | VDDHAN | Power | A | 2.8V Power Supply | |
| 10 | VSSHAN | GND | A | 2.8V GND | |
| 11 | VDDHDA | Power | A | 2.8V Power Supply | NC (*) |
| 12 | VDDMDA | Power | A | 1.8V Power Supply | 1.8V |
| 13 | VDDMIO1 | Power | D | 1.8V Power Supply | |
| 14 | XVS | I/O | D | Digital I/O | |
| 15 | SDA | I/O | D | Digital I/O | I2C pin |
| 16 | SCL | I | D | Digital I/O | I2C pin |
| 17 | INCK | I | D | Digital Input | Clock input |
| 18 | VDDHFIL | Power | A | 2.8V Power Supply | |
| 19 | VDDLSC1 | Power | D | 1.05V Power Supply | |
| 20 | VSSLSC1 | GND | D | 1.05V GND | |
| 21 | VDDLSC2 | Power | D | 1.05V Power Supply | |
| 22 | VSSLSC2 | GND | D | 1.05V GND | |
| 23 | VDDLSC3 | Power | D | 1.05V Power Supply | |
| 24 | VSSLSC3 | GND | D | 1.05V GND | |
| 25 | VDDLSC4 | Power | D | 1.05V Power Supply | |
| 26 | VSSLSC4 | GND | D | 1.05V GND | |
| 27 | VDDMMD | Power | D | 1.8V Power Supply | |
| 28 | D4N | O | D | Digital Output | MIPI output (DATA–) |
| 29 | D4P | O | D | Digital Output | MIPI output (DATA+) |
| 30 | D2N | O | D | Digital Output | MIPI output (DATA–) |
| 31 | D2P | O | D | Digital Output | MIPI output (DATA+) |
| 32 | VSSLSC5 | GND | D | 1.05V GND | |
| 33 | VDDLIF1 | Power | D | 1.05V Power Supply | |
| 34 | CKN | O | D | Digital Output | MIPI output (CLOCK–) |
| 35 | CKP | O | D | Digital Output | MIPI output (CLOCK+) |
| 36 | VDDLIF2 | Power | D | 1.05V Power Supply | |
| 37 | VSSLSC6 | GND | D | 1.05V GND | |
| 38 | D1N | O | D | Digital Output | MIPI output (DATA–) |
| 39 | D1P | O | D | Digital Output | MIPI output (DATA+) |
| 40 | D3N | O | D | Digital Output | MIPI output (DATA–) |



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| No. | Symbol | I/O | A/D | Description | Remarks |
|---|---|---|---|---|---|
| 41 | D3P | O | D | MIPI | MIPI output(DATA+) |
| 42 | VSSLSC7 | GND | D | 1.05V GND | |
| 43 | VDDLSC7 | Power | D | 1.05V Power Supply | |
| 44 | VDDLPL1 | Power | D | 1.05V Power Supply | |
| 45 | VSSLPL1 | GND | D | 1.05V GND | |
| 46 | VDDLPL2 | Power | D | 1.05V Power Supply | |
| 47 | VSSLPL2 | GND | D | 1.05V GND | |
| 48 | VDDLSC8 | Power | D | 1.05V Power Supply | |
| 49 | VSSLSC8 | GND | D | 1.05V GND | |
| 50 | VDDLSC9 | Power | D | 1.05V Power Supply | |
| 51 | VSSLSC9 | GND | D | 1.05V GND | |
| 52 | VDDLSC10 | Power | D | 1.05V Power Supply | |
| 53 | VSSLSC10 | GND | D | 1.05V GND | |
| 54 | VRLRD2 | Minus | A | -1.2V Input | Connect to VRLRD1 ,VRLRD3 and VRLRD4 |
| 55 | VRL2 | Minus | A | -1.2V Input | Connect to VRL1 ,VRL3 and VRL4 |
| 56 | VPISD2 | Power | A | 2.8V Input | Connect to VPISD1 |
| 57 | VPI2 | Power | A | 2.8V Input | Connect to VPI1 |
| 58 | VSSHPX2 | GND | A | 2.8V GND | |
| 59 | VDDHPX2 | Power | A | 2.8V Power Supply | |
| 60 | VDDLSC11 | Power | D | 1.05V Power Supply | |
| 61 | VSSLSC11 | GND | D | 1.05V GND | |
| 62 | VDDLCN1 | Power | D | 1.05V Power Supply | |
| 63 | VSSLCN1 | GND | D | 1.05V GND | |
| 64 | VDDLCN2 | Power | D | 1.05V Power Supply | |
| 65 | VSSLCN2 | GND | D | 1.05V GND | |
| 66 | VSSLCN3 | GND | D | 1.05V GND | |
| 67 | VDDMCM1 | Power | A | 1.8V Power Supply | 1.8V |
| 68 | VDDHCM1 | Power | A | 2.8V Power Supply | NC (*) |
| 69 | VSSHPX3 | GND | A | 2.8V GND | |
| 70 | VDDHPX4 | Power | A | 2.8V Power Supply | |
| 71 | VSSHPX4 | GND | A | 2.8V GND | |
| 72 | VRL3 | Minus | A | -1.2V Input | Connect to VRL1 ,VRL2 and VRL4 |
| 73 | VRLRD3 | Minus | A | -1.2V Input | Connect to VRLRD1 ,VRLRD2 and VRLRD4 |
| 74 | VDDSUB | Power | A | 2.8V Power Supply | |
| 75 | VDDHPX5 | Power | A | 2.8V Power Supply | |
| 76 | VSSHPX5 | GND | A | 2.8V GND | |
| 77 | VSSSUB | GND | D | 1.05V GND | |
| 78 | FSTROBE | O | D | Digital Output | Flash strobe |
| 79 | SLASEL | I | D | Digital Input | Slave address control<br>(pull-down) |
| 80 | GPO | O | D | Digital Output | NC |



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| No. | Symbol | I/O | A/D | Description | Remarks |
|---|---|---|---|---|---|
| 81 | SWDIO | I/O | D | Digital I/O | NC |
| 82 | SWTCK | I | D | Digital Input | NC |
| 83 | TENABLE | I | D | Digital Input | NC(pull-down) |
| 84 | VDDLSC12 | Power | D | 1.05V Power Supply | |
| 85 | VSSLSC12 | GND | D | 1.05V GND | |
| 86 | TEST1 | I | D | Digital Input | NC |
| 87 | TEST2 | I | D | Digital Input | NC |
| 88 | TEST3 | I | D | Digital Input | NC |
| 89 | TESTOUT | O | D | Digital Output | NC |
| 90 | POREN | I | D | Digital Input | NC |
| 91 | XCLR | I | D | Digital Input | |
| 92 | VDDMIO2 | Power | D | 1.8V Power Supply | |
| 93 | VSSHPX6 | GND | A | 2.8V GND | |
| 94 | VDDHPX6 | Power | A | 2.8V Power Supply | |
| 95 | TVMON | O | A | Analog Output | NC |
| 96 | TVCDSIN | I | A | Analog Input | NC |
| 97 | VRLRD4 | Minus | A | -1.2V Input | Connect to VRLRD1 ,VRLRD2 and VRLRD3 |
| 98 | VRL4 | Minus | A | -1.2V Input | Connect to VRL1 ,VRL2 and VRL3 |
| 99 | VSSHPX7 | GND | A | 2.8V GND | |
| 100 | VDDHPX7 | Power | A | 2.8V Power Supply | |
| 101 | VSSHPX8 | GND | A | 2.8V GND | |
| 102 | VDDHCM2 | Power | A | 2.8V Power Supply | NC (*) |
| 103 | VDDMCM2 | Power | A | 1.8V Power Supply | 1.8V |
| 104 | VSSLCN4 | GND | D | 1.05V GND | |
| 105 | VSSLCN5 | GND | D | 1.05V GND | |
| 106 | VDDLCN5 | Power | D | 1.05V Power Supply | |
| 107 | VSSLCN6 | GND | D | 1.05V GND | |
| 108 | VDDLCN6 | Power | D | 1.05V Power Supply | |
| 109 | VSSLSC13 | GND | D | 1.05V GND | |
| 110 | VDDLSC13 | Power | D | 1.05V Power Supply | |

Note : The pin shall be "NC(No Connection)" in this case(VANA2=1.8V)



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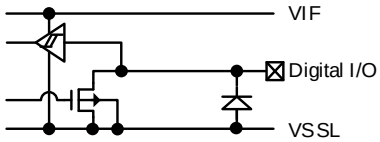
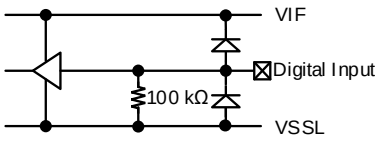
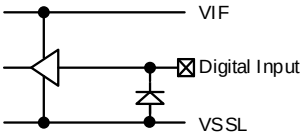
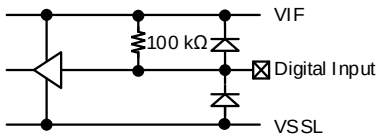
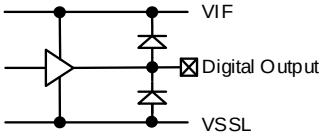
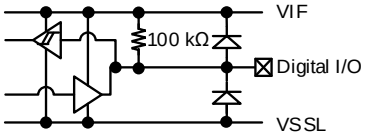
## Input / Output Equivalent Circuit

| Symbol | Equivalent Circuit | Symbol | Equivalent Circuit |
|---|---|---|---|
| SCL<br>SDA |  | SLASEL |  |
| INCK |  | XCLR |  |
| GPO<br>FSTROBE |  | XVS |  |

VIF : 1.8 V power supply
VSSL : VDIG GND

**Figure 2 Input / Output Equivalent Circuit**



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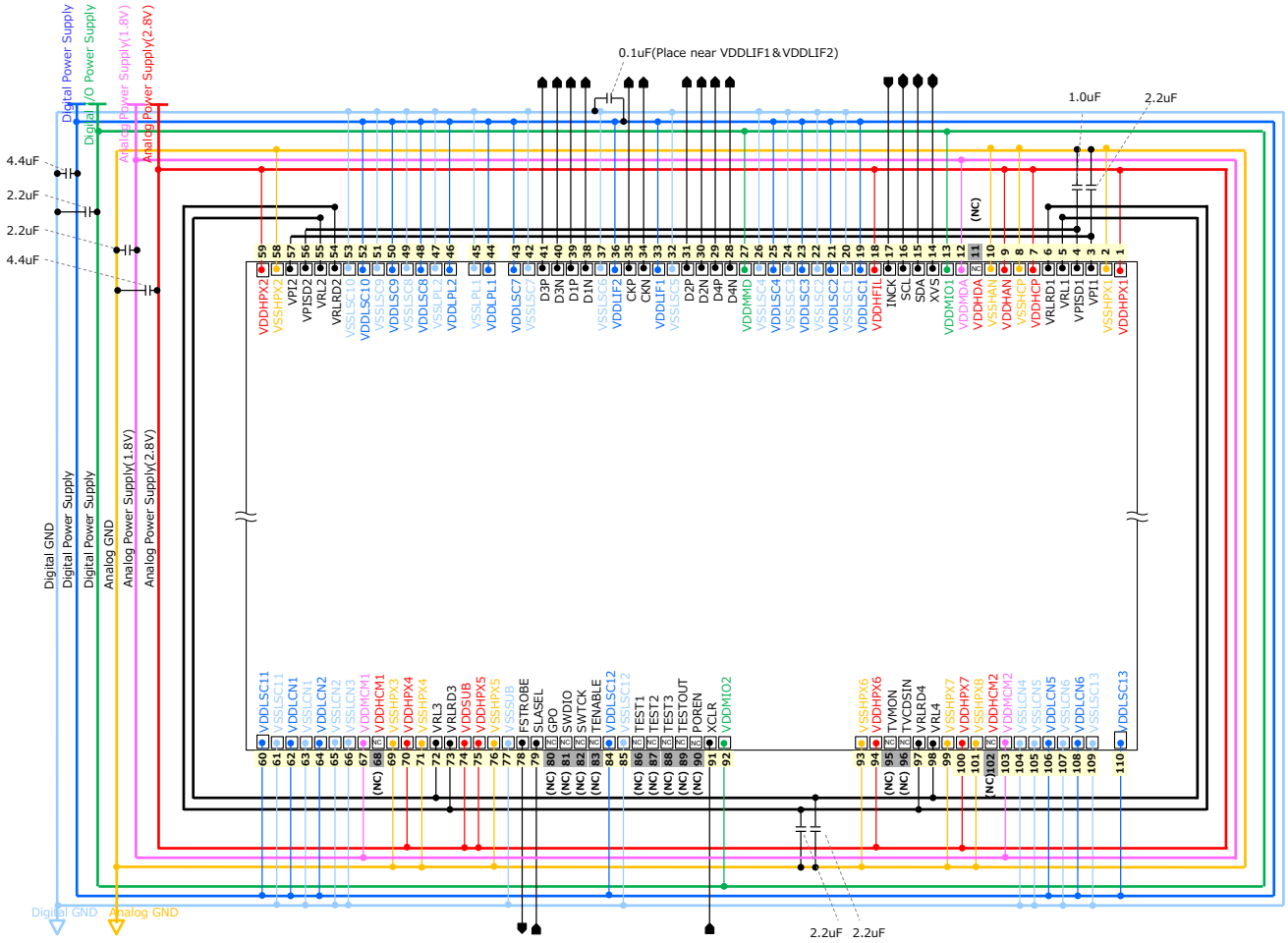
## Peripheral Circuit Diagram

Case1:Analog 2.8V and 1.8V

VPI Internal use is recommended.




Note: The capacitor values and parts count used for decoupling of power supply lines in this diagram are determined only with Sony Semiconductor Solutions Corporation's testing environment. The capacitor values and/or parts count for power line decoupling may have to be reviewed and optimized by each manufacture depending on their design.

**Figure 3 Reference circuit schematicsVPI1,2 (pixel power supplies) are internally supplied.**

Case 2 : Analog 2.8V only (as an option)

See Figure A-1.



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## Functional Description

### System Outline

IMX363-AAQH5-C is a CMOS active pixel type image sensor which adopts the Exmor RS technology to achieve high sensitivity, low noise, and high speed image capturing. It is embedded with backside illuminated imaging pixel, low noise analog amplifier, column parallel A/D converters which enables high speed capturing, digital amplifier, image binning circuit, timing control circuit for imaging size and frame rate, CSI2 image data high speed serial interface, PLL oscillator, and serial communication interface to control these functions.
Several additional image processing functions and peripheral circuits are also included for easy system optimization by the users.

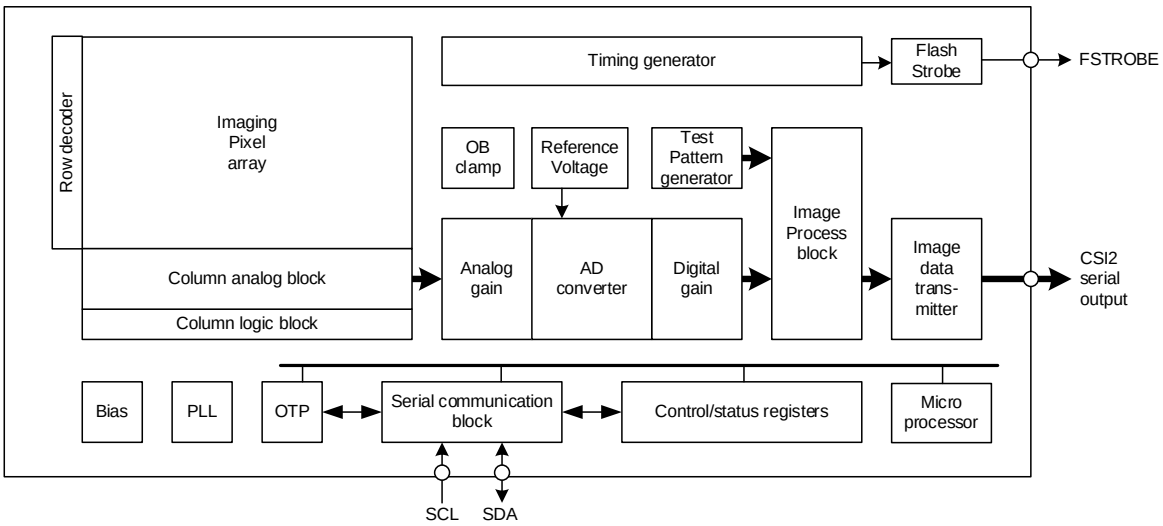


**Figure 4 Overview of functional block diagram**



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## Control register setting by the serial communication

The IMX363-AAQH5-C can use the 2-wire serial communication method for sensor control. These specifications are described for sensor control using the 2-wire serial communication as follows. See Application Notes for more details of each function beyond the following description.

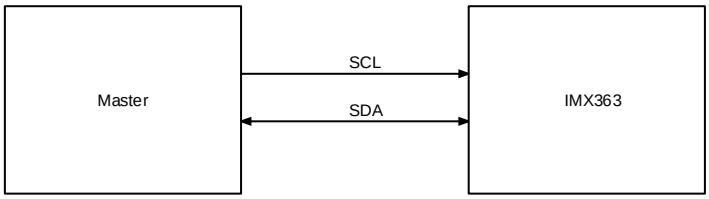


**Figure 5 2-wire serial communication**

## 2-wire Serial Communication Operation Specifications

The 2-wire serial communication method conforms to the Camera Control Instance (CCI). CCI is an I2C compatible interface, and the data transfer protocol is I2C standard. IMX363-AAQH5-C supports two transfer speed mode (Fast-mode ≤400KHz, Fast-mode Plus ≤1MHz).
This 2-wire serial communication circuit can be used to access the control-registers and status-registers of IMX363-AAQH5-C.

**Table 3 Description of 2-wire Serial Communication Pins**

| pin name | description |
|---|---|
| SDA | Serial data input/output pin |
| SCL | Serial clock input pin |

The control registers and status registers of IMX363-AAQH5-C are mapped on the 16-bit address space.
The register categories shown below. Detail register information is shown in each chapter/section in this document and in Register Map.

**Table 4 Specification of register address map for 2-wire serial communication**

| | address range | description | Note |
|---|---|---|---|
| $I^2C$ register | 0x0000 - 0x0fff | Configuration register<br>Read Only and Read/Write Dynamic register | |
| | 0x1000 - 0x1fff | Parameter limit register<br>Read Only static resister | |
| | 0x2000 - 0x2fff | Reserved | |
| | 0x3000 - 0x31ff | Manufacture specific register | Customer register |
| | 0x3200 - 0xffff | Manufacturer specified register | Internal register |



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## Communication Protocol

2-wire serial communication supports a 16-bit register address and 8-bit data message type.

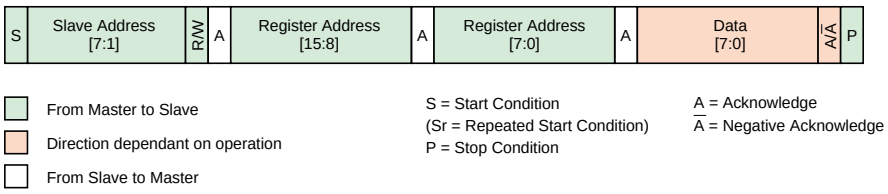


**Figure 6　2-wire serial communication protocol**

IMX363-AAQH5-C has a default slave address shown as below.
The slave address is selectable by pin connection of SLASEL.
When called by the selected slave address, serial communication interface is activated.
Duplication of the address on the same bus must be prevented.
*For other slave address options, refer to Application Note.

| Slave address (Write or Read) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit [7:0] | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0* | Type | Value | SLASEL |
| Bit value | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | Write | 0x34 | L or NC |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | Read | 0x35 | |

| Bit [7:0] | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0* | Type | Value | SLASEL |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit value | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Write | 0x20 | H |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Read | 0x21 | |

* Note : Bit[0] is R/W setting bit, see Table 5

R/W shows the direction of communication.

**Figure 7　Slave address**

**Table 5　R/W bit**

| R/W bit | direction of communication | address |
|---|---|---|
| 0 | Write (Master → Sensor) | 0: 0x20 or 0x34 |
| 1 | Read (Sensor → Master) | 1: 0x21 or 0x35 |



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## Clock generation and PLL

IMX363-AAQH5-C equips embedded PLL to generate the necessary internal clocks and CSI2 transmission clocks. Set the related registers according to the operation condition. See Application Notes for more details of each function.

## Clock System Diagram

IMX363-AAQH5-C is equipped with 2 PLLs, one to output VTCK for image processing, and the other to output OPCK for MIPI output. The VTCK PLL can output at 375 to 1260 MHz, and the OPCK PLL can output at 1000 to 2150 MHz, based on a clock input with the 9 to 27 MHz range.
The VTCK PLL could be configured with divider of up to 1/1 to 1/4 range, and multiply in the 32 to 210 range.
The OPCK PLL could be configured with divider of up to 1/1 to 1/4 range, and multiply in the 84 to 358 range.
IMX363-AAQH5-C normally recommend to make it operate in dual PLL mode by driving both PLLs, however can also operate in single PLL mode by driving just one PLL from parameter setting flexibility point of view. In PLL single mode, PREPLLCK_OP_DIV and PLL_OP_MPY are ignored.

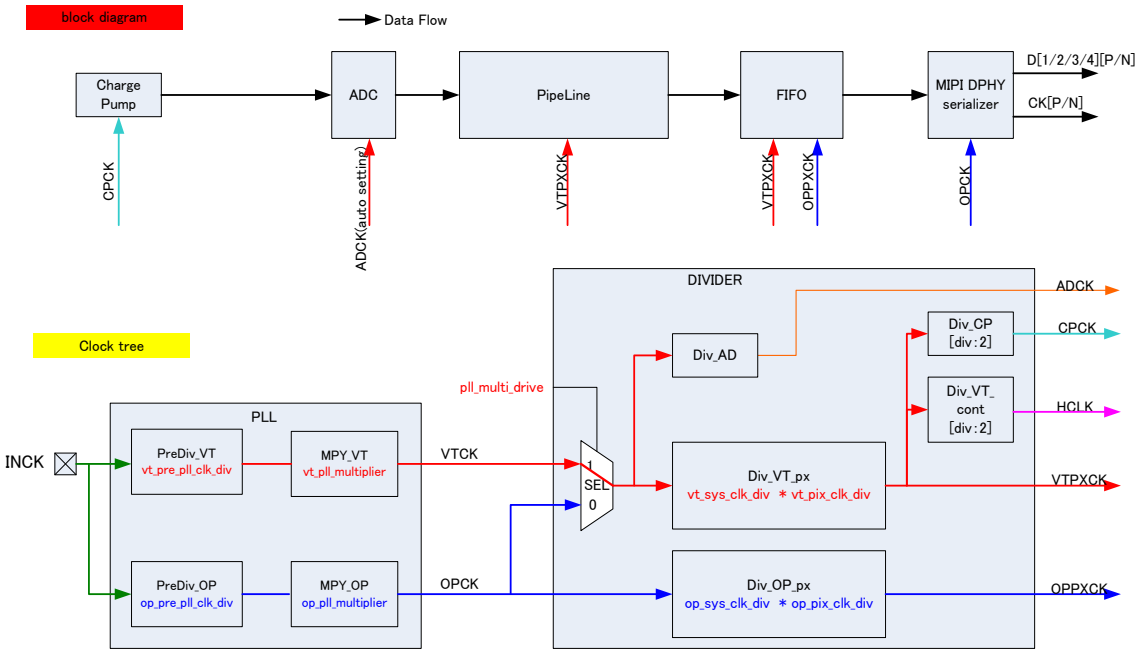


**Figure 8 Clock System Diagram (PLL dual mode)**



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## Description of operation clocks

The followings are general descriptions for each clock. See Application Note for more detail.

### INCK

INCK is an external input clock (9 to 27MHz). See “AC characteristics” for electrical requirements to INCK.

### VTCK, OPCK : PLL output

These clocks are the root of all the operation clocks in IMX363-AAQH5-C and it designates the data rate. CKP/CKN; CSI2 interface clock is generated from OPCK by dividing into 1/2 frequency since the interface is operated in double data rate format.

### VTPXCK Clock

The clock for internal image processing is generated by dividing into 1/6, 1/8, 1/10, 1/12, 1/14, 1/16, 1/18, 1/20, 1/24, 1/28, 1/32, 1/36 or 1/40 frequency. This clock is used as the base of integration time, frame rate, and etc.

### OPPXCK Clock

The clock for internal image processing is generated by dividing into 1/6, 1/8, 1/10, 1/12, 1/16, 1/20 or 1/24 frequency according to the word length of the CSI2 interface. This clock is designating the pixel rate and etc.



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## Image Readout Operation

By setting the parameters of PLL, image size, start/end position of the imaging area, direction of reading image, binning, shutter mode, integration time, gain, and output format via 2-wire serial communication, IMX363-AAQH5-C outputs the image data.

See Application Notes for more details of each function.

## Physical alignment of imaging pixel array

The figure below shows the physical alignment of the imaging pixel array with pin #1 located at the upper right corner.

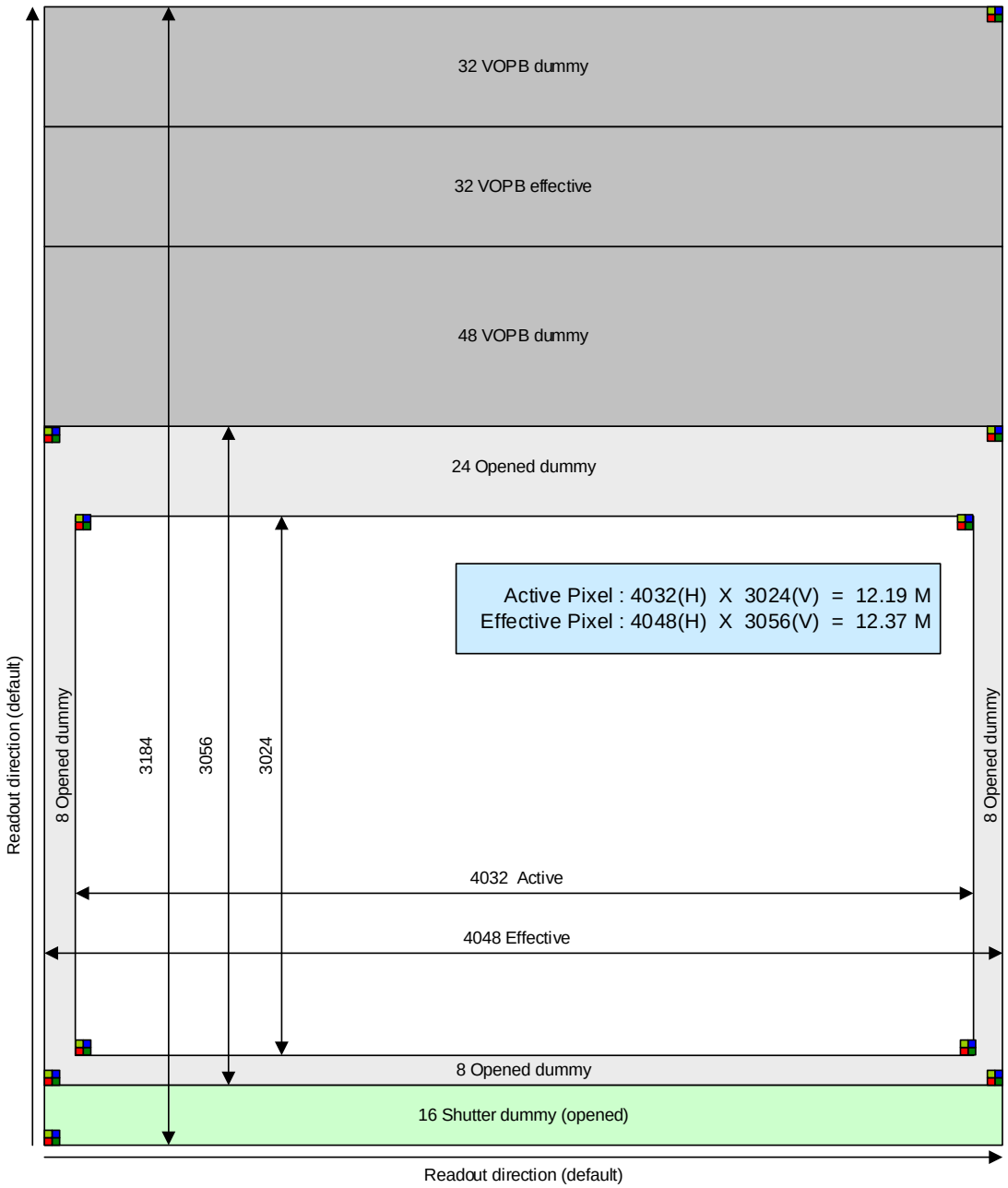


**Figure 9 physical alignment of the imaging pixel array**



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### Color coding and order of reading image date

The original color filter arrangement of the sensor is shown in the figure below. Gr and Gb are the G signals shown at the same line as R signals and B signals, respectively. The line with R & Gr signals and the line with Gb & B signals are output one after the other alternatively. Each pixel consists of Left sub-pixel and Right sub-pixel. There are read out mode which output summed sub-pixel data (Mode2/3/4). These data are read out in order as shown in the figure below.

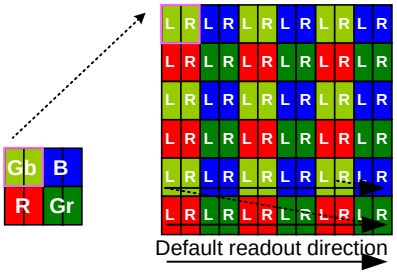


**Figure 10 Color coding alignment**

### Output Image Format

This is the output image diagram of full pixel output mode, Image data is output from the upper left corner of the diagram.

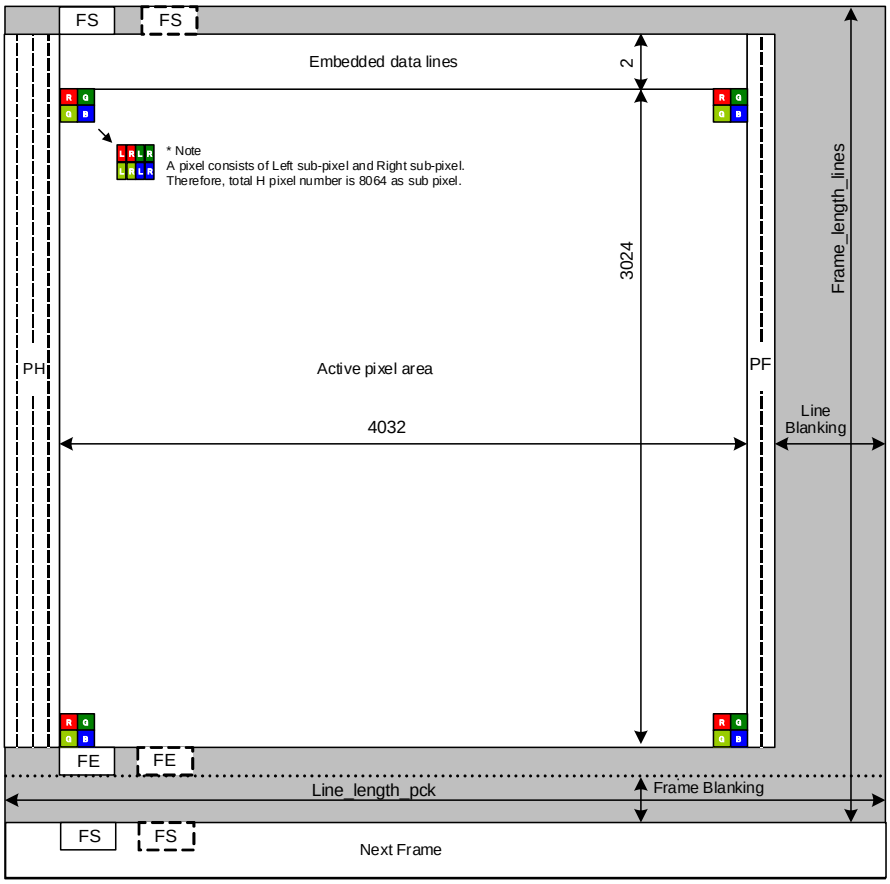


**Figure 11 Full pixel output mode data structure**



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### Embedded Data Line control

It is possible to output certain 2-wire serial register contents on the 2 lines just after the FS sync code of the frame. Undefined value is output when not outputting embedded data. See Application Notes for contents and output sequence of Embedded Data Lines.

### Dual PD technology

IMX363-AAQH5-C has 12 Mega pixels with pair of 1.4x0.7um rectangle pixel.
Each pixel consists of Left sub-pixel, Right sub-pixel, one OCL, one Color Filter and no Metal shield.
Left sub-pixel is similar to Right Shield pixel. And also, Right sub-pixel is similar to Left Shield pixel.
Since all of pixels obtain Left image data and Right image data, it's possible to create phase information from all of active area to achieve high speed and highly accurate PDAF system.

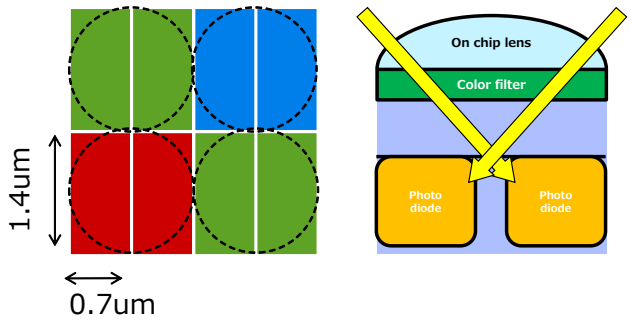


**Figure 12 Structure of sensor**

### Dual PD Output Mode

IMX363-AAQH5-C has 3 modes of Dual PD output mode.
See Application Notes for details.

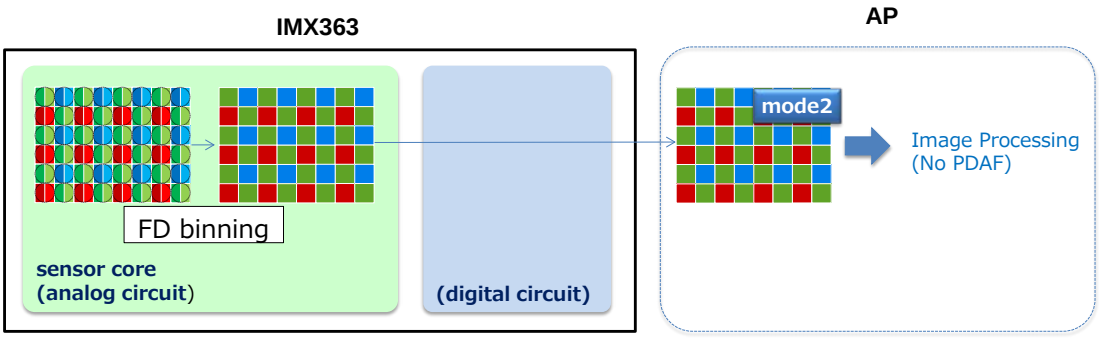


**Figure 13 Dual PD output mode2**



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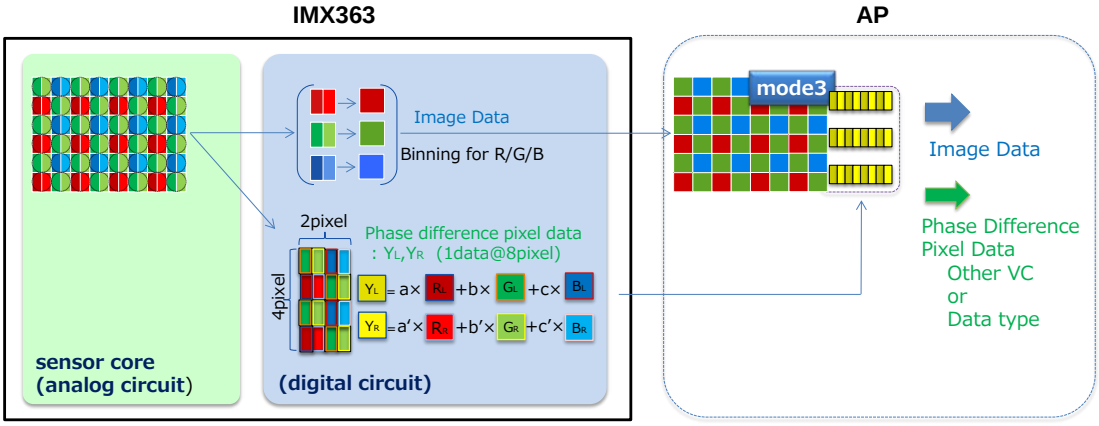


**Figure 14 Dual PD output mode3**

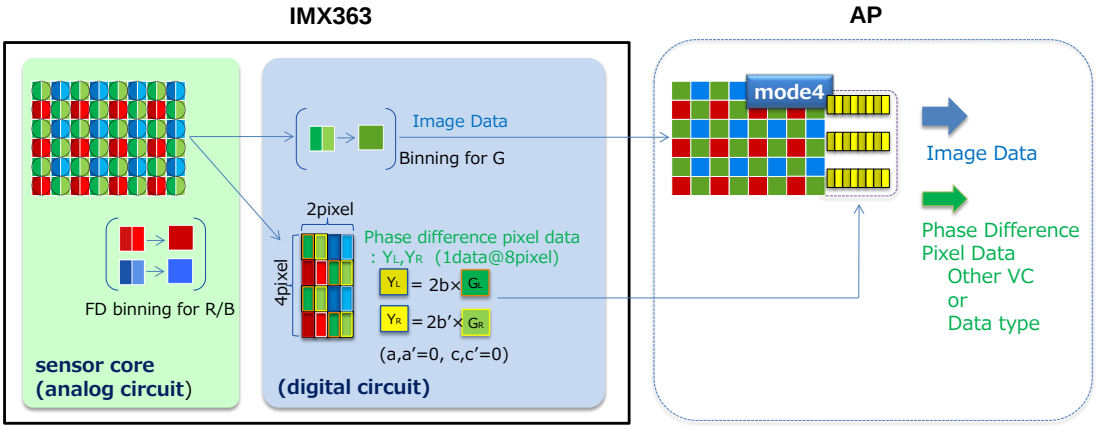


**Figure 15 Dual PD output mode4**



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### Phase difference pixel data control

IMX363-AAQH5-C supports Phase difference pixel data generation in mode3/4 and outputs as a packet different from normal image data.
Visible Pixel Data and Phase difference pixel data go out alternately as shown below figure.
Phase difference pixel data packet is identified by defining VC ID or data type in the data ID packet.
See Application Notes for details.

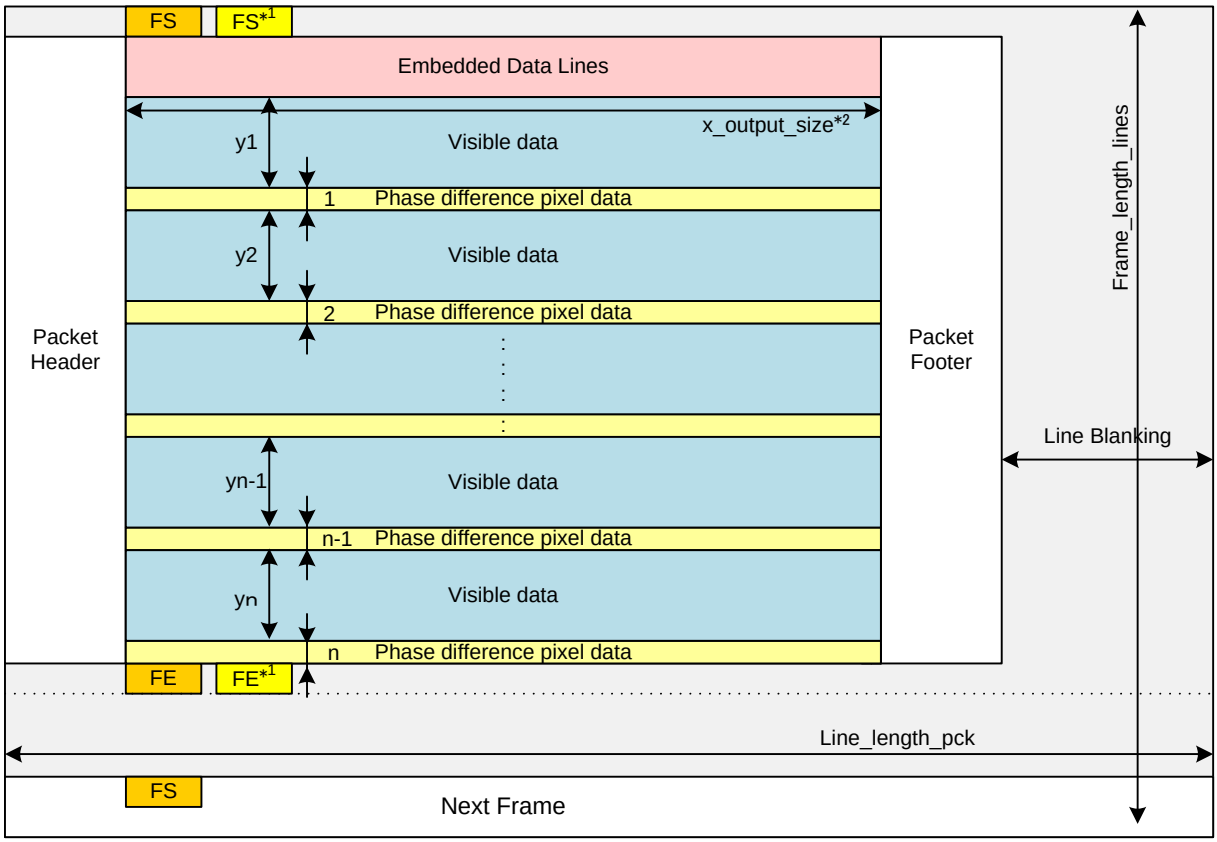


**Figure 16 Phase difference pixel data output mode data structure**



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## Image size of mode

IMX363-AAQH5-C can capture and output full size, cropped/scaled image in combination with the normal mode or HDR mode. Examples are shown in the table below. Definitions of each parameter are shown in the below figure. Image output size depends on sensor operation mode. See Application Notes for details.

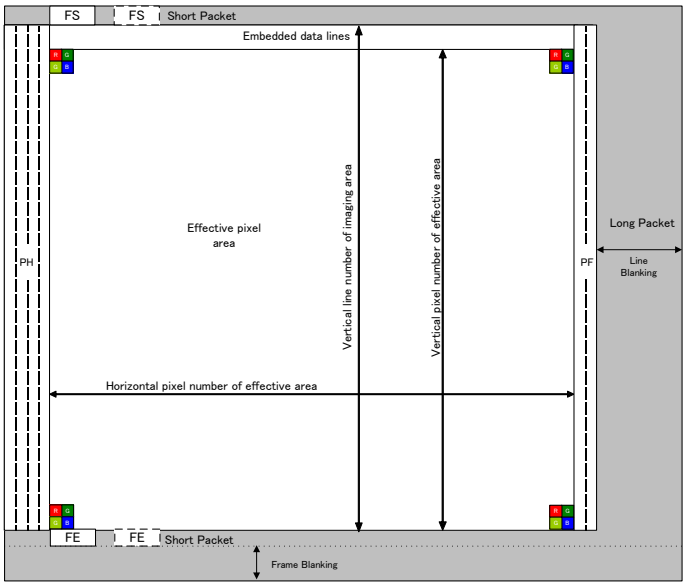


**Figure 17 Image size parameter definition**

**Table 6 modes and image sizes (normal)**

| Capture Mode | Normal capture mode | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Image Size Mode | Full | | | 4K2K | | | FHD | | | HD | | | WVGA | | |
| Aspect Ratio | 4:3 | | | 16:9 | | | 16:9 | | | 16:9 | | | 16:9 | | |
| Analog Cropping | - | | | - | | | V crop | | | V crop | | | V crop | | |
| Digital Cropping | - | | | - | | | - | | | - | | | - | | |
| Analog Binning | - | | | - | | | V 2bin | | | H 2bin , V 2bin | | | H 2bin , V 2bin | | |
| Digital Binning | - | | | - | | | H 2bin | | | - | | | H 2bin | | |
| Analog Subsampling | - | | | - | | | - | | | - | | | V 2sub | | |
| Digital Subsampling | - | | | - | | | - | | | - | | | - | | |
| Dual PD Output Mode | Mode2 | Mode3 | Mode4 | Mode2 | Mode3 | Mode4 | Mode2 | Mode3 | Mode4 | Mode2 | Mode3 | Mode4 | Mode2 | Mode3 | Mode4 |
| Number of horizontal pixels in effective area* | 4032 | 4032 | 4032 | 4032 | 4032 | 4032 | 2016 | 2016 | 2016 | 2016 | 2016 | 2016 | 1008 | 1008 | 1008 |
| Number of vertical lines in effective area | 3024 | 3024 | 3024 | 2272 | 2272 | 2272 | 1136 | 1136 | 1136 | 1136 | 1136 | 1136 | 568 | 568 | 568 |
| Frame Rare | 30 | 30 | 30 | 60 | 30 | 60 | 120 | 90 | 90 | 240 | 120 | 120 | 480 | 180 | 180 |
| Horizontal size of Phase Difference data | - | 4032 | 4032 | - | 4032 | 4032 | - | 2016 | 2016 | - | 2016 | 2016 | - | 1008 | 1008 |
| Vertical size of Phase Difference data | - | 756 | 756 | - | 568 | 568 | - | 284 | 284 | - | 284 | 284 | - | 142 | 142 |
| FOV | | | | | | | | | | | | | | | |
| Output | | | | | | | | | | | | | | | |



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**Table 7　modes and image sizes (HDR)**

| Capture Mode | HDR capture mode | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Image Size Mode | Full | | | 4K2K | | | FHD | | | HD | | | WVGA |
| Aspect Ratio | 4:3 | | | 16:9 | | | 16:9 | | | 16:9 | | | - |
| Analog Cropping | - | | | V crop | | | V crop | | | V crop | | | - |
| Digital Cropping | - | | | - | | | - | | | - | | | - |
| Analog Binning | - | | | - | | | V 2bin | | | V 2bin | | | - |
| Digital Binning | - | | | - | | | - | | | - | | | - |
| Analog Subsampling | - | | | - | | | - | | | - | | | - |
| Digital Subsampling | - | | | - | | | - | | | - | | | - |
| Dual PD Output Mode | Mode2 | Mode3 | Mode4 | Mode2 | Mode3 | Mode4 | Mode2 | Mode3 | Mode4 | Mode2 | Mode3 | Mode4 | - |
| Number of horizontal pixels in effective area* | 4032 | 4032 | 4032 | 4032 | 4032 | 4032 | 4032 | 4032 | 4032 | 4032 | 4032 | 4032 | - |
| Number of vertical lines in effective area | 3024 | 3024 | 3024 | 2272 | 2272 | 2272 | 1136 | 1136 | 1136 | 1136 | 1136 | 1136 | - |
| Frame Rare | 30 | 30 | 30 | 60 | 30 | 60 | 120 | 90 | 90 | 120 | 90 | 120 | - |
| Horizontal size of Phase Difference data | - | 4032 | 4032 | - | 4032 | 4032 | - | 4032 | 4032 | - | 4032 | 4032 | - |
| Vertical size of Phase Difference data | - | 756 | 756 | - | 568 | 568 | - | 284 | 284 | - | 284 | 284 | - |
| FOV | | | | | | | | | | | | | - |
| Output | | | | | | | | | | | | | - |

*Note: In mode2/3/4, output data unit is pixel (summed data of Left and Right sub-pixel). See Figure 13,14,15.



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## Description about operation mode

IMX363-AAQH5-C corresponds Normal image and Single Frame High Dynamic Range (HDR) image output. There are five image size mode in Normal, four image size mode in HDR. Also each image size has for operation modes. Please refer Table6 and Table7.

## Image area control capabilities

As control function for image's viewing area and /or image size, IMX363-AAQH5-C has capability of analog crop, digital crop and output crop. The relation of image output size and the resister is shown below.

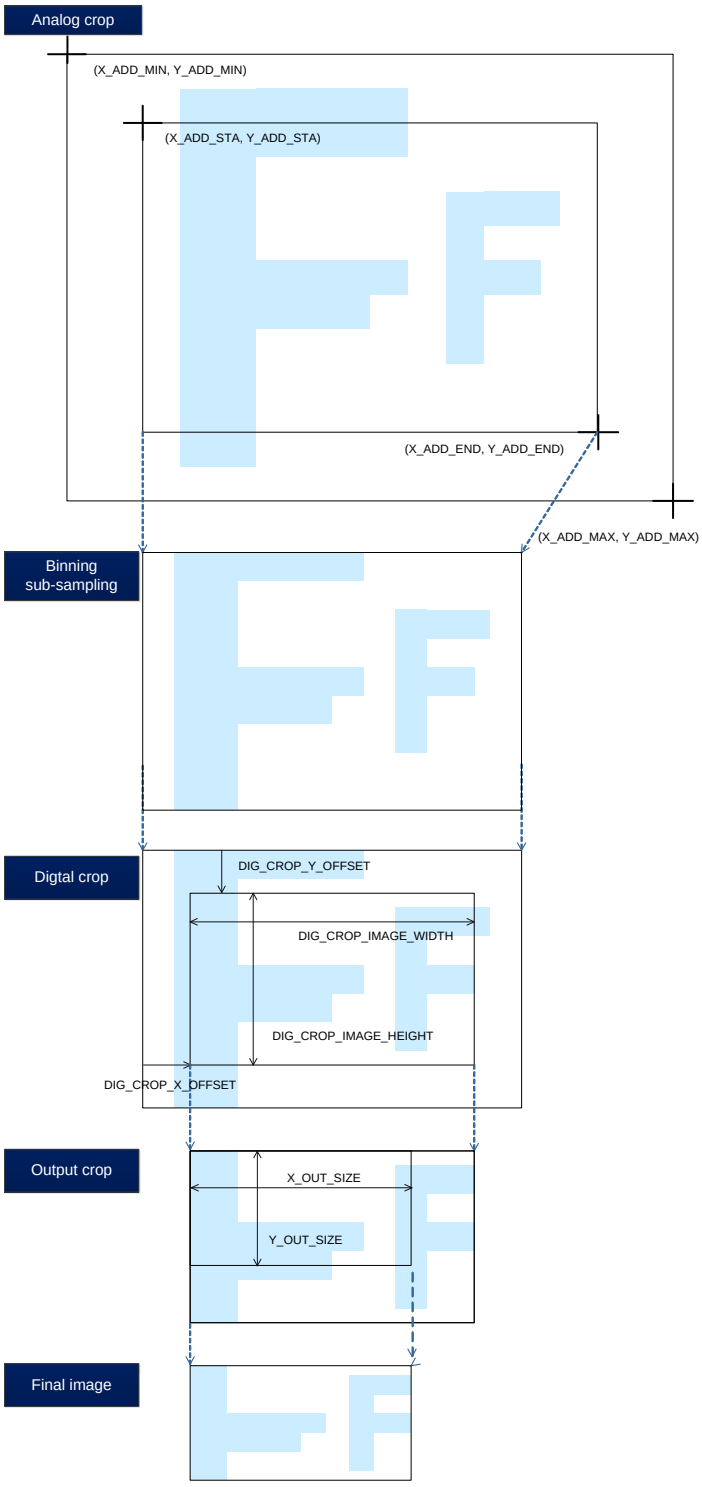


**Figure 18 image area control capabilities**



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### Readout Start Position

Default readout position of IMX363-AAQH5-C starts from the lower left whenever PIN1 is placed at the upper right corner. Because the lens will invert the image both vertically and horizontally, the proper image can be achieved when PIN1 is placed at the upper right corner.

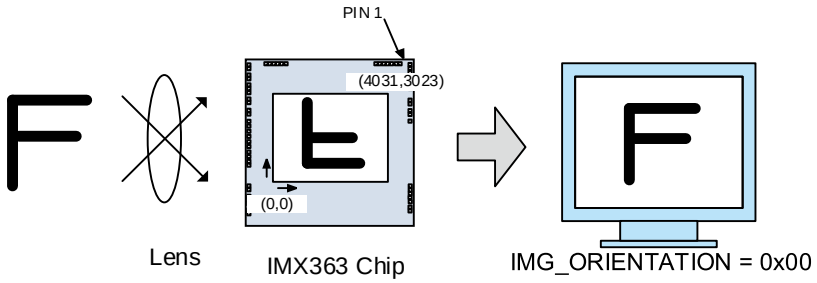


**Figure 19 Readout start position**

Vertical flip and horizontal mirror readout modes can be specified by the register below. When the readout direction is changed, the color of the first pixel (R/Gr/Gb/B, Left/Right read out also changes with it. In the Normal mode, the first pixel is Left/Red or Left/Green.
In the Mirror mode , the first pixel is Right/Blue or Right/Green.

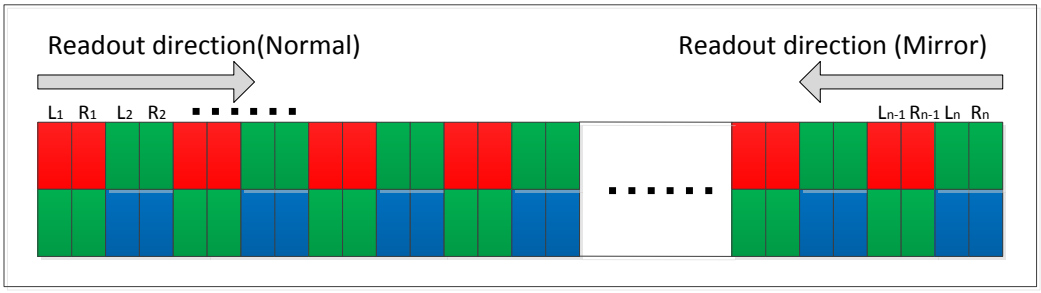


**Figure 20 Readout direction**

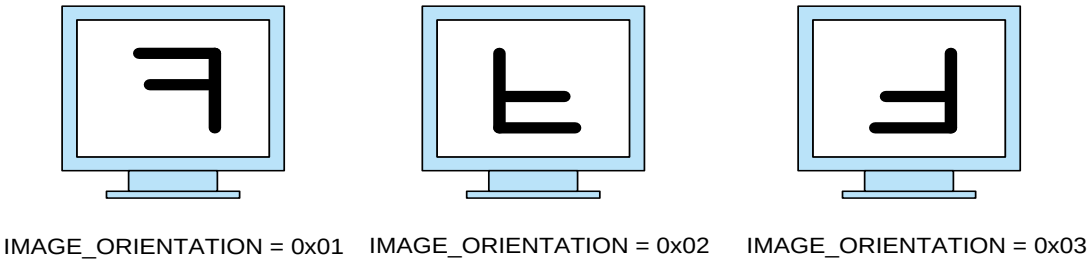


**Figure 21 Read out image for each combination of flip and mirror**



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### Gain setting

IMX363-AAQH5-C can apply analog gain on photo-electron signal and digital gain on digital signal after ADC. Range of settable range is as follows.

**Table 8 Range of Gains**

| Function | Max. |
|---|---|
| Analog Gain | 18dB |
| Digital Gain | 24dB |

### Image compensation function

There are some additional functions in sensor image pipeline. Use-case may be chosen in terms of trade-off for power consumption and image quality for example.

See Application Notes for more details of each function.

#### Defect Pixel Correction

The defect correction function includes static defect correction and dynamic defect correction.

The static defect correction is to correct the defective pixels according to address data stored in OTP. There are two areas; one for Sony Semiconductor Solutions Corporation's factory area, another for module vendors.
The dynamic defect correction eliminates any critical defects detected on RGB pixel array by estimating from surrounding adjacent pixels value.

#### Chroma Noise Reduction (CNR)

IMX363-AAQH5-C does not support Chroma Noise Reduction (CNR).

#### Luminance Noise Reduction (LNR)

IMX363-AAQH5-C does not support Luminance Noise Reduction (LNR).



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## Miscellaneous functions

IMX363-AAQH5-C has the following additional functions to be used for various final products' features.

See Application Notes for more details of each function.

### Thermal Meter

This function is to measure the thermal data from internal sensor then average it. Measurement results could be read via I2C or EBD data.

### Test pattern output and type of test pattern

IMX363-AAQH5-C can output test pattern of SMIA specification by build-in pattern generator.
Test patterns of Solid Color, 100% Color Bar, Fade to Gray Color Bar and PN9 are available.
For Solid Color mode, each value of R, Gr, Gb and B is adjustable.

### OTP (One Time Programmable Read Only Memory)

Total of 29K bit of OTP is available for users. It is divided into 55 pages and most of them are usable at user's discretion while 53th and 54th pages are assigned as the area for defective pixel correction, SMIA model ID, and partially write protected. See OTP manual for details.

### Flash light control sequence

IMX363-AAQH5-C can internally generate the control pulse assuming to trigger the flash light emission and output from the external pins (FSTROBE).

### External pixel power supply capability

IMX363-AAQH5-C can select internal connection or external power supply for pixels. Sony Semiconductor Solutions Corporation's recommendation is "internal connection". Corresponding supply pins are VPI1 and VPI2. The selection of internal or external shall be made by register setting. See IMX363-AAQH5-C Module Design Reference Manual for more detail.

## Image signal interface

### MIPI transmitter

IMX363-AAQH5-C outputs image signal by CSI2 high speed serial interface consisted of one pair of clock line and four pairs of data line. See MIPI Alliance Standard for Camera Serial Interface2 (CSI-2) version 1.2 and MIPI Alliance Specification for D-PHY version 1.2 for details.

Because signal is transmitted by differential pair, impedance (generally 100 Ω) between differential pair near the receiver side during HS mode is required. Otherwise, select receiver with build-in impedance between differential pair. Different delay time of differential pairs may reduce the input timing margin of ISP device, which leads to malfunction. Therefore, delay time within and among differential pairs must be as similar as possible in layout.



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# How to operate IMX363-AAQH5-C

## Power on sequence

### Power on slew rate

Maximum and minimum slew rate (mV / µs) is specified for each power supply to avoid oscillation during a power-on sequence.

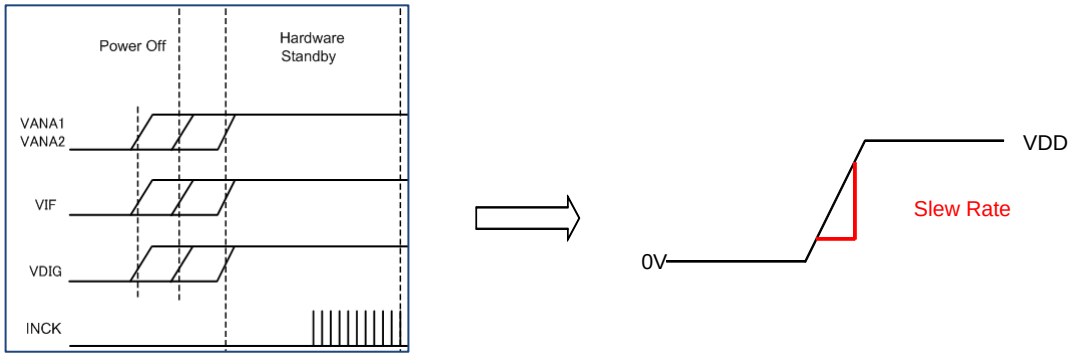


**Figure 22 Power on slew rate**

**Table 9 Limitation on power-on slew rate**

| Power Supplies | Slew Rate | | | Comment |
|---|---|---|---|---|
| | Min | Max | Unit | |
| VANA1,VANA2,VIF<br>VDIG | 7 | 100 | mV/µs | |



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### Startup sequence with 2-wire serial communication

Time constraints exist between power-on release timing and XCLR release timing when external XCLR control is used.
Please follow the power supply start up sequence below.

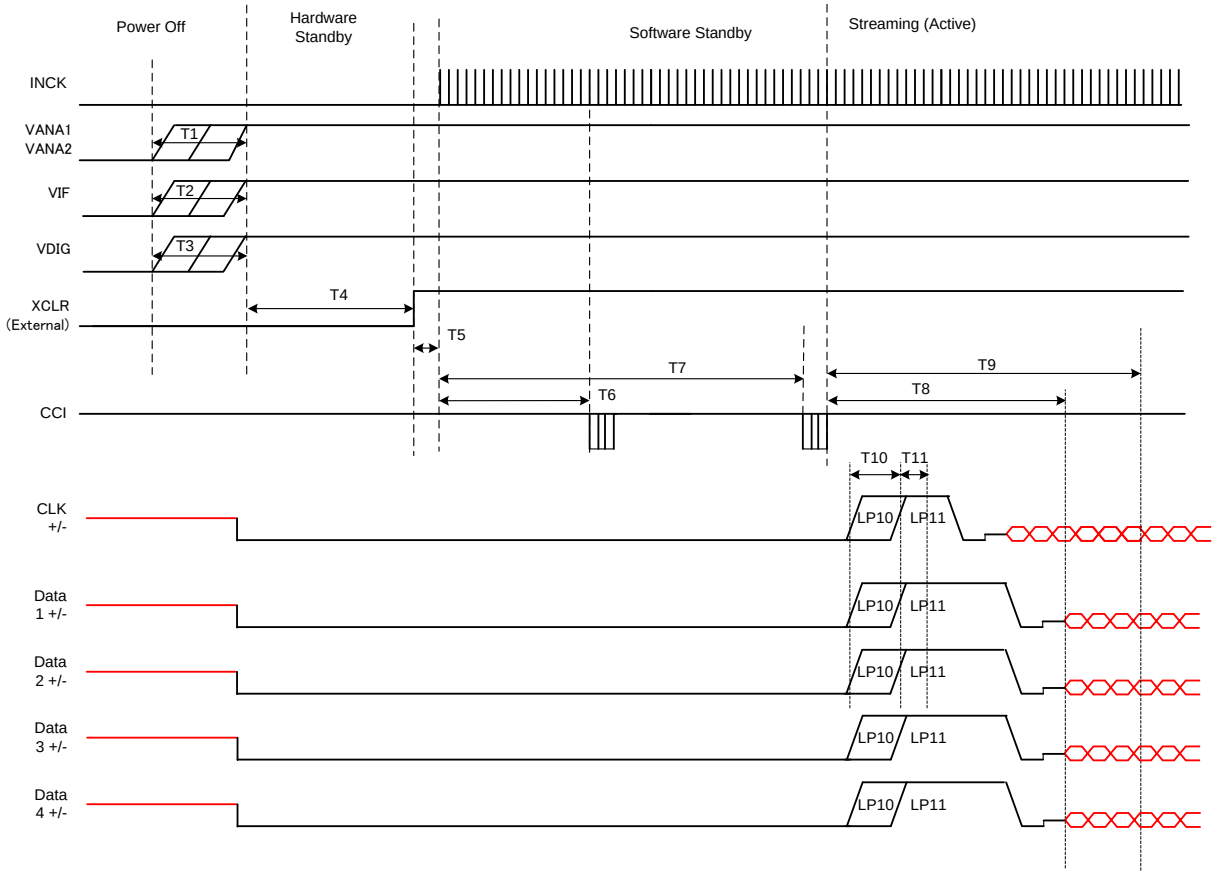


**Figure 23 Start up sequence with 2-wire serial communication (external reset)**

* Presence of INCK during Power Off is acceptable despite of above chart.



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**Table 10 Startup sequence timing constraints (2-wire serial communication mode with external reset)**

| Item | Label | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|
| VANA1,VANA2 rising – VANA1,VANA2 on | T1 | VANA1, VANA2, VDIG and VIF may rise in any order. | | µs | Slew rate of VANA1,VANA2, VDIG and VIF (0%-100%):max100mv/us |
| VDIG rising – VDIG on | T2 | | | µs | |
| VIF rising – VIF on | T3 | | | µs | |
| VANA1,VANA2, VDIG and VIF rising– XCLR rising | T4 | 0 | | µs | Later of T1, T2, T3 |
| XCLR rising till INCK input | T5 | 250 | | µs | |
| INCK rising till CCI Read Version ID register wait time | T6 | 1 | | ms | |
| INCK rising till Send Streaming Command wait time (To complete reading all parameters from NVM) | T7 | 24 (INCK:9MHz)<br>11 (INCK:19.2MHz)<br>9 (INCK:24MHz)<br>8 (INCK:26MHz) | | ms | (VRL cap : 2.2µF) |
| | T8 | | 3 ms + The delay of the coarse integration time value +128H | | |
| Entering Streaming Mode – First Frame Start Sequence of good quality frame in first power up including initialization delays. All frames outputted shall have good quality. | T9 | | T8 + 1Frame | Frames | |
| DPHY power up | T10 | 1 | 1.1 | ms | |
| DPHY init | T11 | 100 | 110 | µs | |

Note) XCLR needs to be Low until all power supplies complete power-on.



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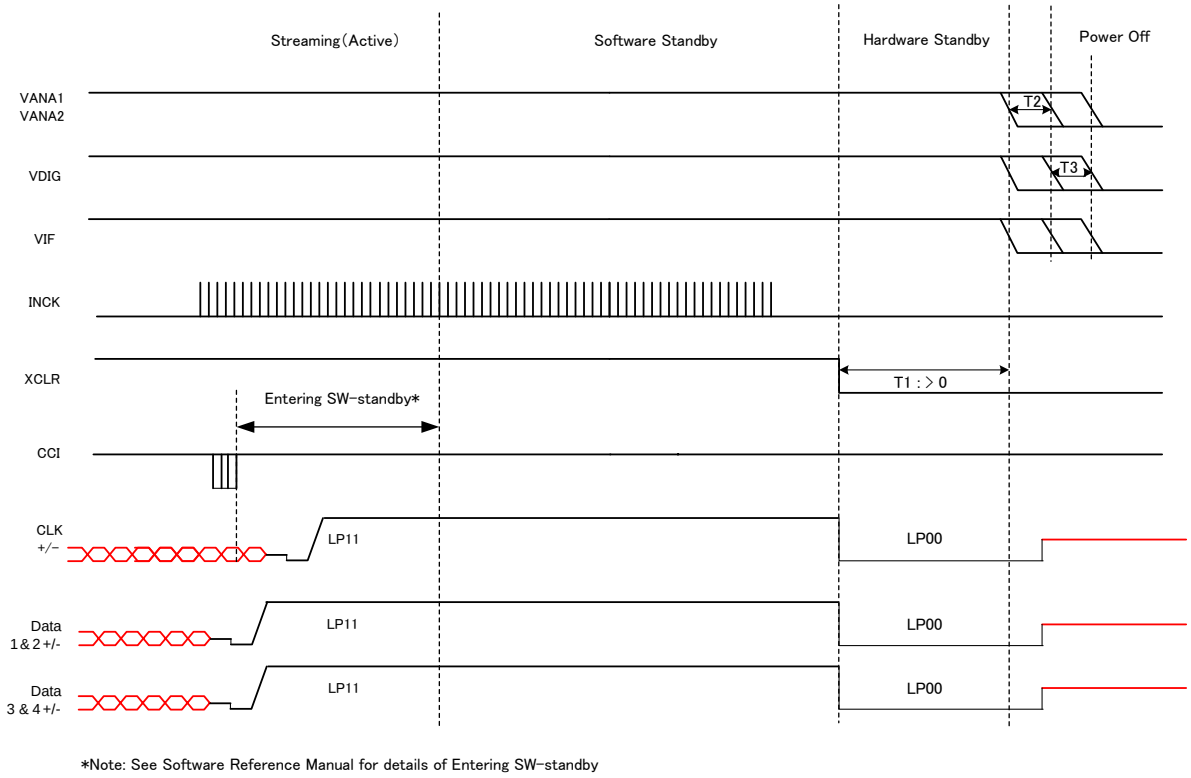
## Power down sequence

### Power down sequence with 2-wire serial communication

Time constraints exist between power-down release timing and XCLR release timing when external XCLR control is used.
Follow the power down sequence below.




*Note: See Software Reference Manual for details of Entering SW-standby

**Figure 24 Power down sequence with 2-wire serial communication (external reset)**

**Table 11 Power down sequence timing constraints (2-wire serial communication mode with external reset)**

| Item | Label | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|
| XCLR negedge - VANA (VDIG or VIF) fall | T1 | 0 | | ns | |
| Sequence free of VANA falling and VDIG falling and VIF falling | T2, T3 | VANA1,VANA2, VDIG and VIF may fall in any order. | | ns | |

## Register Map

See Register Map.



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## Electrical Characteristics

The Electrical Characteristics of the IMX363-AAQH5-C is shown below

### DC characteristics

**Table 12 DC Characteristics (Analog 2.8V and 1.8V operation)**

| Item | Pins | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Supply voltage | VDDHPX1,2,4,5,6,7 | VANA1 | 2.8V supply | 2.7 | 2.8 | 2.9 | V |
| | VDDHCM1,2 | | | | | | |
| | VDDHAN | | | | | | |
| | VDDHDA | | | | | | |
| | VDDHFIL | | | | | | |
| | VDDSUB | | | | | | |
| | VDDHDA | VANA2 | (*) | N.C. | N.C. | N.C. | |
| | VDDHCM1,2 | | | | | | |
| | VDDMDA | | 1.8V supply | 1.7 | 1.8 | 1.9 | |
| | VDDMCM1,2 | | | | | | |
| | VDDMIO1,2, VDDMMD | VIF | | 1.7 | 1.8 | 1.9 | V |
| | VDDLCN1,2,5,6 | VDIG | | 0.95 | 1.05 | 1.15 | V |
| | VDDLSC1,2,3,4,7,8,9, 10,11,12,13 | | | | | | |
| | VDDLIF1,2 | | | | | | |
| | VDDLPL1,2 | | | | | | |
| Digital input voltage | SDA, SCL | VIH | | 0.7VIF | | 2.9 | V |
| | | VIL | | -0.3 | | 0.3VIF | V |
| Digital input voltage | XCLR, INCK SLASEL XVS | VIH | | 0.65VIF | | VIF + 0.3 | V |
| | | VIL | | -0.3 | | 0.35VIF | V |
| Digital output voltage | SDA, FSTROBE XVS | VOH | | VIF-0.4 | | | V |
| | | VOL | | | | 0.4 | V |

Note : The pin shall be "NC(No Connection)" in this case(VANA2=1.8V)



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## AC Characteristics

### Master Clock Waveform Diagram

#### INCK Square Waveform Input Specifications

Input specifications are shown below when square-wave signal is input directly into the external pin INCK.

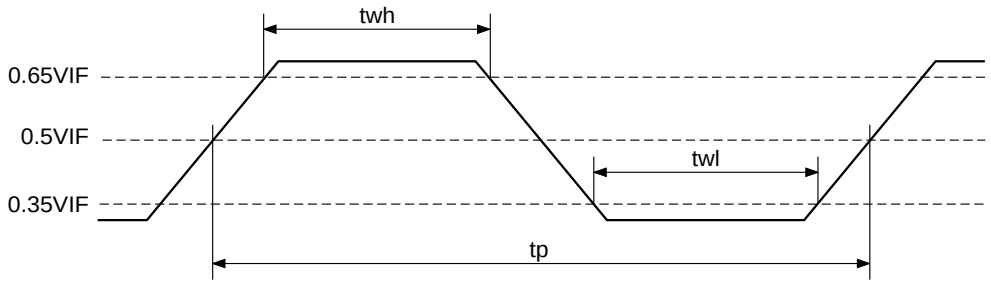


**Figure 25 Master Clock Square Waveform Input Diagram**

**Table 13 Master Clock Square Waveform Input Characteristics**

| PARAMETER | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| INCK clock frequency | $f_{SCK}$ | 9 | | 27 | MHz |
| INCK clock period | $t_p$ | 37 | | 111 | ns |
| INCK low level width | $t_{wl}$ | 0.4tp | | 0.6tp | ns |
| INCK high level width | $t_{wh}$ | 0.4tp | | 0.6tp | ns |
| INCK jitter | Tjitter | | | 600 | ps |

#### INCK Sine Waveform Input Specifications

IMX363-AAQH5-C does not support the “AC coupled connection”.
Therefore, there is no description of AC characteristics

### PLL block characteristics

Electrical characteristics of PLL block is shown below.

**Table 14 PLL block characteristics (VT system)**

| Item | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Input frequency range | 9.0 | | 27.0 | MHz | |
| Input frequency range of phase comparator | 6 | | 12.0 | MHz | |
| VCO frequency range | 750.0 | | 1260.0 | MHz | |
| Output frequency range | 375.0 | | 1260.0 | MHz | |
| Settling time | | | 1000.0 | µs | |

Conditions) VANA1 = 2.8 V, VANA2 = 1.8 V, VDIG = 1.05 V, Tj = 25 ˚C.



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**Table 15 PLL block characteristics (OP system)**

| Item | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Input frequency range | 9.0 | | 27.0 | MHz | |
| Input frequency range of phase comparator | 6.0 | | 12.0 | MHz | |
| VCO frequency range | 1000.0 | | 2150.0 | MHz | |
| Output frequency range | 1000.0 | | 2150.0 | MHz | |
| Settling time | | | 1000.0 | μs | |

Conditions) $V_{ANA1}$ = 2.8 V, $V_{ANA2}$ = 1.8 V, $V_{DIG}$ = 1.05 V, Tj = 25 ˚C, Output frequency = 2150 MHz.



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### Definition of settling time of PLL block

After start operation, the oscillation frequency of PLL output transits from 0 Hz to target frequency then gradually become stable. The duration for oscillation frequency becomes within 5 % of the target frequency is defined as “settling time”.

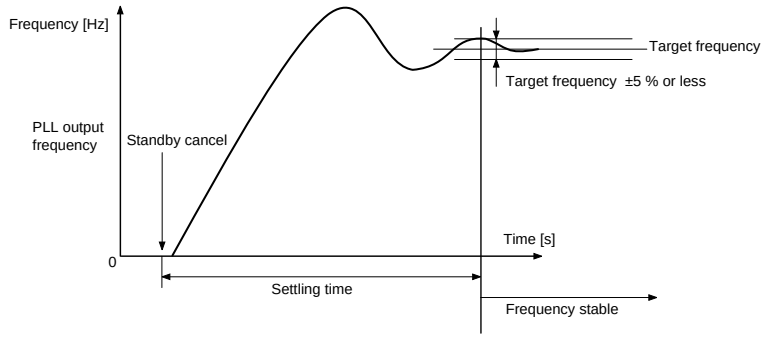


**Figure 26 Definition of settling time**

### 2-wire serial communication block characteristics

2-wire serial communication characteristics are shown below.
IMX363-AAQH5-C supports I2C Fast-Mode Plus.

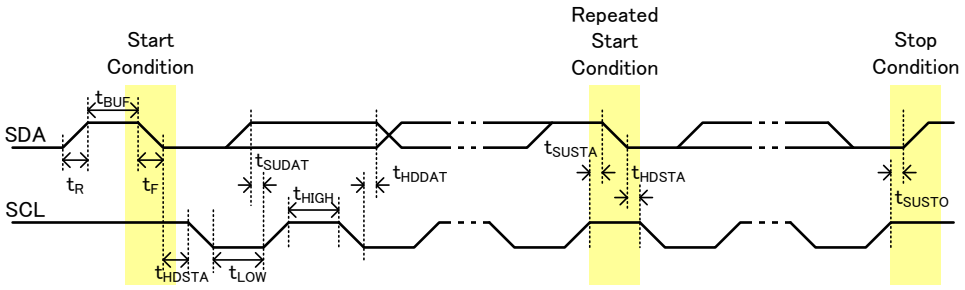


**Figure 27 2-wire serial communication block specification**

**Table 16 2-wire serial communication block specification**

| Parameter | Symbol | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Low level input voltage | $V_{IL}$ | | -0.3 | $0.3V_{IF}$ | V |
| High level input voltage | $V_{IH}$ | | $0.7V_{IF}$ | 2.9 | V |
| Low level output voltage | $V_{OL1}$ | VIF > 2 V, Sink 3 mA | 0 | 0.4 | V |
| | $V_{OL2}$ | VIF ≤ 2 V, Sink 3 mA | 0 | $0.2V_{IF}$ | V |
| High level output voltage | $V_{OH}$ | | $V_{IF}$ - 0.4 | | V |
| Low level output current | $I_{OL}$ | $V_{OL}$ = 0.4V | 20 | | mA |
| Output fall time | $t_{of}$ | Load 10 pF – 400 pF, 0.7 VIF→0.3 VIF | | 250 (120)* | ns |
| Input current | $I_I$ | 0.1 VIF→0.9 VIF | -10 | 10 | μA |
| SDA I/O capacitance | $C_{I/O}$ | | | 8 | pF |
| SCL Input capacitance | $C_I$ | | | 6 | pF |

*Note: Fast-mode Plus



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**Table 17 2-wire serial communication block AC specification**

**Fast-mode**

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| SCL clock frequency | $f_{SCL}$ | 0 | 400 | kHz |
| Rise time (SDA and SCL) | $t_R$ | — | 300 | ns |
| Fall time (SDA and SCL) | $t_F$ | — | 300 | ns |
| Hold time (start condition) | $t_{HDSTA}$ | 0.6 | — | µs |
| Setup time (rep.-start condition) | $t_{SUSTA}$ | 0.6 | — | µs |
| Setup time (stop condition) | $t_{SUSTO}$ | 0.6 | — | µs |
| Data setup time | $t_{SUDAT}$ | 100 | — | ns |
| Data hold time | $t_{HDDAT}$ | 0 | 0.9 | µs |
| Bus free time between Stop and Start condition | $t_{BUF}$ | 1.3 | | µs |
| Low period of the SCL clock | $t_{LOW}$ | 1.3 | | µs |
| High period of the SCL clock | $t_{HIGH}$ | 0.6 | | µs |

**Fast-mode Plus**

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| SCL clock frequency | $f_{SCL}$ | 0 | 1000 | kHz |
| Rise time (SDA and SCL) | $t_R$ | — | 120 | ns |
| Fall time (SDA and SCL) | $t_F$ | — | 120 | ns |
| Hold time (start condition) | $t_{HDSTA}$ | 0.26 | — | µs |
| Setup time (rep.-start condition) | $t_{SUSTA}$ | 0.26 | — | µs |
| Setup time (stop condition) | $t_{SUSTO}$ | 0.26 | — | µs |
| Data setup time | $t_{SUDAT}$ | 50 | — | ns |
| Data hold time | $t_{HDDAT}$ | 0 | | µs |
| Bus free time between Stop and Start condition | $t_{BUF}$ | 0.5 | | µs |
| Low period of the SCL clock | $t_{LOW}$ | 0.5 | | µs |
| High period of the SCL clock | $t_{HIGH}$ | 0.26 | | µs |



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## Current consumption and standby current

**Table 18 Current consumption and standby current**

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Current consumption (analog) | $I_{ANA1}$ | - | 30.1 | 40.8 | mA | |
| Current consumption (analog) | $I_{ANA2}$ | - | 31.2 | 38.5 | mA | |
| Current consumption (digital) | $I_{DIG}$ | - | 143.7 | 216.2 | mA | |
| Current consumption (IF) | $I_{IF}$ | - | 2.9 | 3.6 | mA | |
| Standby current (analog1) | $I_{STBANA1}$ | - | - | 32.1 | μA | XCLR :Low fixed<br>INCK :stop |
| Standby current (analog2) | $I_{STBANA2}$ | - | - | 1.0 | μA | XCLR :Low fixed<br>INCK :stop |
| Standby current (digital) | $I_{STBDIG}$ | - | - | 28.3 | mA | XCLR :Low fixed<br>INCK :stop |
| Standby current (IF) | $I_{STBIF}$ | - | - | 29.7 | μA | XCLR :Low fixed<br>INCK :stop |

Note) Mode3 Full HDR ,30 frame/s, DPC=OFF
VANA1 = 2.8 V, VANA2 = 1.8 V, VDIG = 1.05 V, VIF = 1.8 V, Tj = 60 ˚C



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## Spectral Sensitivity Characteristic

(Includes neither lens characteristics nor light source characteristics.)

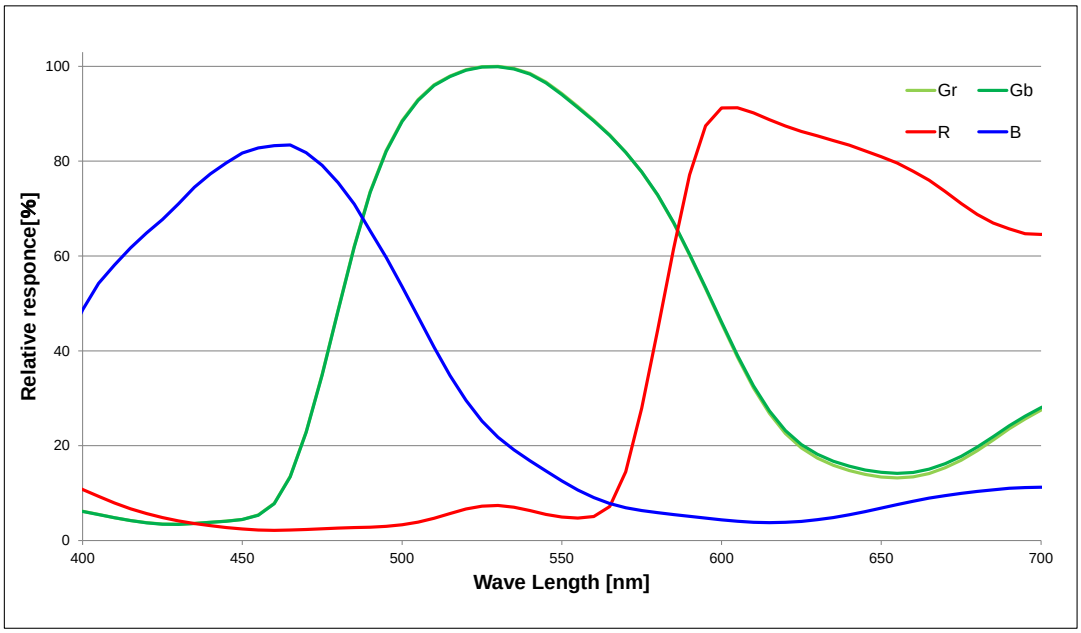


**Figure 28 Spectral sensitivity characteristics**



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## Image Sensor Characteristics

### Image Sensor Characteristics

**Table 19 Image Sensor Characteristics**

(30 frame/s, $V_{ANA1}$ = 2.8 V, $V_{ANA2}$ = 1.8 V, $V_{DIG}$ = 1.05 V, $V_{IF}$ = 1.8 V,Tj = 60 ˚C)

| Item | Symbol | Min. | Typ. | Max. | Unit | Range | Measurement method | Remarks |
|---|---|---|---|---|---|---|---|---|
| Sensitivity | S | 241 | | | LSB | Center | 1(*1) | 1/120 s storage |
| Sensitivity ratio | RG | 0.46 | 0.51 | 0.57 | | Center | 2(*1) | |
| | BG | 0.38 | 0.43 | 0.48 | | | | |
| Saturation signal | Vsat | 1023 | | | LSB | Zone1 | 3(*1) | Include OB level(*2) |
| Video signal shading | SH | | | 80 | % | Zone2D | 4(*1) | |
| Dark signal | Vdt | | | 0.5 | LSB | Zone2D | 5(*1) | |

The data described at this image sensor characteristics are the measurement standard without base gain setting, and indicates the results evaluated with OB as a reference.

Note 1) These refer to the descriptions of the section “Measurement Method”.

Note 2) LSB is the abbreviation of Least Significant Bit. 10 bits = 1023 digital is the maximum output code for the output unit. The gain setting (base gain setting) in which the saturation signal output matches with 1023 LSB requires 0[dB] when the OB level is 64 LSB (standard recommended value).

### Zone Definition used for specifying image sensor characteristics

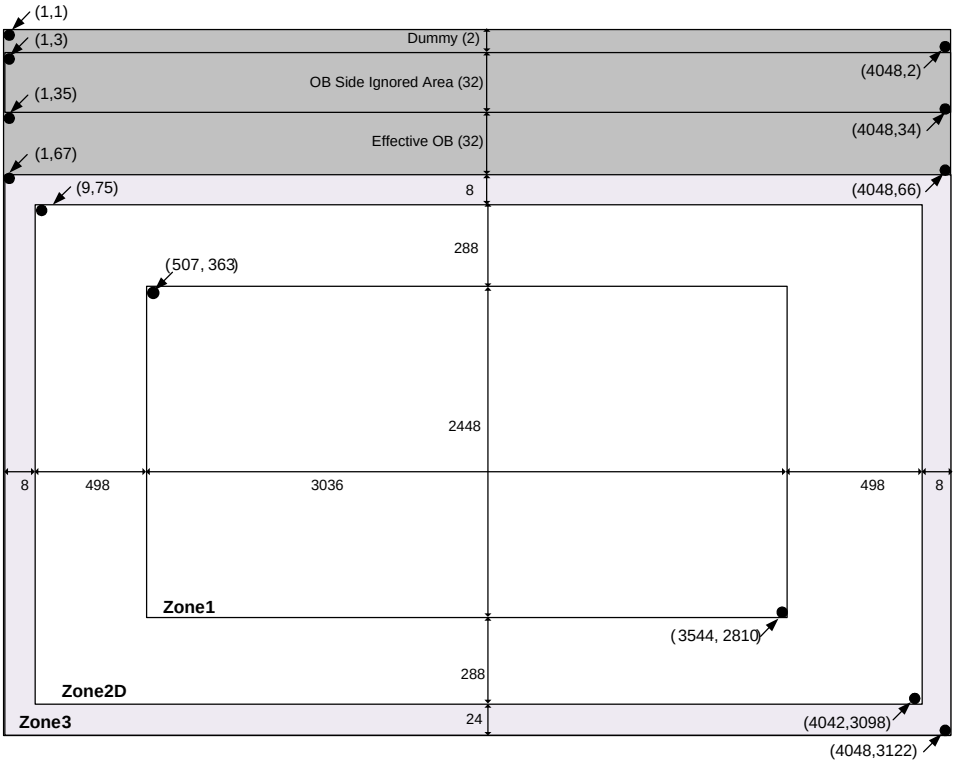


**Figure 29 Zone Definition Diagram**



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## Measurement Method for Image Sensor Characteristics

### Measurement conditions

The device operation conditions are at the typical values of the bias and clock voltage.

**Table 20 Measurement Conditions**

| | |
|---|---|
| Supply voltage | Analog(VANA1) 2.8 V, Analog(VANA2) 1.8V, digital 1.05 V, IF 1.8 V |
| Clock | INCK 18 MHz |

In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr, Gb, R and B digital signal outputs of the measurement system.

### Color Coding of This Image Sensor and Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively. The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.
All pixel signals are output successively in a 1/15 s period.

**Figure 30 Color coding alignment**

### Definition of Standard Imaging Conditions

#### Standard imaging condition I

Use a pattern box (luminance: 706 cd/m2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F2.8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

#### Standard imaging condition II

A testing lens with CM500S (t = 1.0 mm) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output, lens aperture or storage time control by the electronic shutter.



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## Measurement method

### 1. Sensitivity

Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/300 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of imaging area, and substitute the values into the following formula.

S = {((VGr + VGb) /2) × (300/120)} [LSB]

### 2. Sensitivity ratio

Set the measurement condition to the standard imaging condition II. After adjusting so that the average value of the Gr and Gb signal output is 300 LSB, measure the R signal output (VR [LSB]), the Gr and Gb signal outputs (VGr, VGb [LSB]) and the B signal output (VB [LSB]) at the imaging area Center in frame readout mode, and substitute the values into the following formulas.

VG = (VGr + VGb) /2

RG = VR/VG

RB = VB/VG

### 3. Saturation signal

Set the measurement condition to the standard imaging condition II. After adjusting the luminous Intensity to 20 times the intensity with the average value of the Gr, Gb signal outputs, 300 [LSB], measure the average value of the Gr, Gb, R and B signal outputs.

### 4. Video signal shading

Set the measurement condition to the standard imaging condition II. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 300 [LSB].
Then measure the maximum value (Gmax [LSB]) and minimum value (Gmin [LSB]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

SH = ((Gmax – Gmin) /Gmax) × 100 [%]

### 5. Dark signal

Measure the output difference between 1/15 [s] signal output (Va) and 1/15000 or less [s] signal output (Vb) at the device ambient temperature of 60 ˚C and the device in the light-obstructed state, and calculate the signal output at 1/15 [s] storage by them using the following approximate formula. Then, this is Vdt [LSB].

Vdt = (Va – Vb) × (1/15) / (1/15) – (1/15000) ≈ (Va –Vb) [LSB]



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## Spot Pixel Specification

(15 frame/s, VANA1= 2.8 V, VANA2= 1.8 V, VDIG = 1.05 V, VIF = 1.8 V, Tj = 60 ˚C)

**Table 21 Spot Pixel Specifications**

| Type of distortion | Level Note 1) | Maximum distorted pixels in each zone | | | | Measurement method | Remarks |
|---|---|---|---|---|---|---|---|
| | | Zone2D | Zone3 | Ineffective OB | Effective OB | | |
| Black or white pixels at high light | 30 % ≤ D | 120 | No evaluation criteria applied | | | SPS_1 | |
| White pixels in the dark | 28 (LSB) ≤ D | 1800 | No evaluation criteria applied | | | SPS_2 | 1/30 storage Note 2) |

Note) 1. D...Spot pixel level.
2. Continuous same color pixels in the horizontal or vertical direction are NG.
3. Defect pixels are measured with all optional image processing features (DPC, HDR) disabled.
4. The maximum quantity pixel counts of 120 for Bright Pixels and 1800 for Dark Pixels are total of R + Gr + Gb + B individual pixels from any color channels.
5. The analog gain for both the Illuminated and Dark defect conditions is 0dB.
6. The above chart (hereinafter referred to as the “Spot Pixel Specifications”) is the standard only for sorting image sensor products in this specification book (hereinafter referred to as the “PRODUCTS”) before shipment from a manufacturing factory. Sony Semiconductor Solutions Corporation and its distributors (collectively hereinafter referred to as the “Seller”) disclaim and will not assume any liability even if actual number of distorted pixels of the PRODUCTS delivered to you exceeds the maximum number set forth in the Spot Pixel Specifications. You are solely liable for any claim, damage or liability arising from or in connection with such distorted pixels. If the Seller separately has its own product warranty program for the PRODUCTS (the “Program”), the conditions in this specification book shall prevail over the Program and the Seller shall not assume any liability under the Program to the extent there is contradiction.



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## Notice on White Pixels Specifications

After shipment inspection of CMOS image sensors, pixels of CMOS image sensors may be distorted and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels.")
Particle radiation such as cosmic rays etc. is one of the causes of White Pixels.
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such distorted pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against White Pixels, such as adoption of automatic compensation systems for White Pixels and establishment of quality assurance standards.
White Pixels may be also caused by alpha radiation, which will be emitted in a process of decay of radioactive isotopes which inevitably exist in the air in minute amounts and may exist in materials or parts of CMOS image sensor devices (e.g. packaging materials, seal glass, wiring materials and IC chips). It is recommended that you should use materials or parts which do not include radioactive isotopes, which are sources of alpha radiation, and consider taking measures, such as adoption of vacuum packaging technologies in order to ensure that the PRODUCTS are not exposed to the air. As the density of radioactive isotopes in the air of the underground space may become thicker than that on the ground, it is highly recommended to ensure the PRODUCTS are not exposed to the air in using or storing the PRODUCTS at the underground space.

**[For Your Reference]**

**The Annual number of White Pixels Occurrence Caused by Particle Radiation such as cosmic rays etc.**

The data in the below chart shows the estimated annual number of White Pixels occurrence caused by particle radiation such as cosmic rays etc. in a single-story building in Tokyo at an altitude of 0 meters. The data shows estimated number of White Pixels based on records of past field tests calculated taking structures and electrical properties of each device into account. However, the data in the chart is for your reference purpose only, and shall not be construed as part of any CMOS image sensor product specifications which the Seller warrants.

**Example of Annual Number of Occurrence**

| White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C) | Annual number of occurrence |
|---|---|
| 15.0 LSB or higher | 1.3 pcs |
| 26.8 LSB or higher | 0.8 pcs |
| 64.2 LSB or higher | 0.4 pcs |
| 133.8 LSB or higher | 0.2 pcs |
| 192.7 LSB or higher | 0.2 pcs |

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the annual number of White Pixels occurrence.

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**Measurement Method for Spot Pixels**

Measure under the standard imaging condition II.

## Spot Pixel Pattern Specifications

### SPS_1. Black or white pixels at high light

After adjusting the average value of the Gr/Gb signal output to 367 LSB, measure the local dip point (black pixel at high light, VXB) and peak point (white pixel at high light, VXK) in the Gr/Gb/R/B signal output Vx (x = Gr/Gb/R/B), and substitute the values into the following formula.
The 367 LSB does not include the dark level offset of 64. The average value is calculated using the signal level output of Zone 2D.

$$D_K(\text{White Pixel level}) = (V_{XK}/\overline{V_X}) \times 100[\%]$$

$$D_B(\text{Black Pixel level}) = (V_{XB}/\overline{V_X}) \times 100[\%]$$

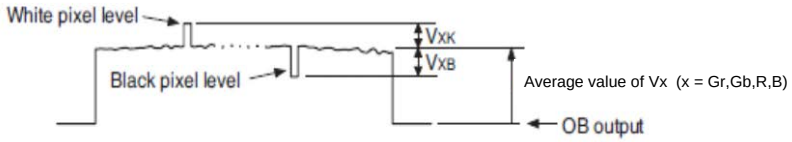


**Figure 31 Measurement Method for Spot Pixels**

### SPS_2 White pixels in the dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.



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## CRA Characteristics of Recommended Lens

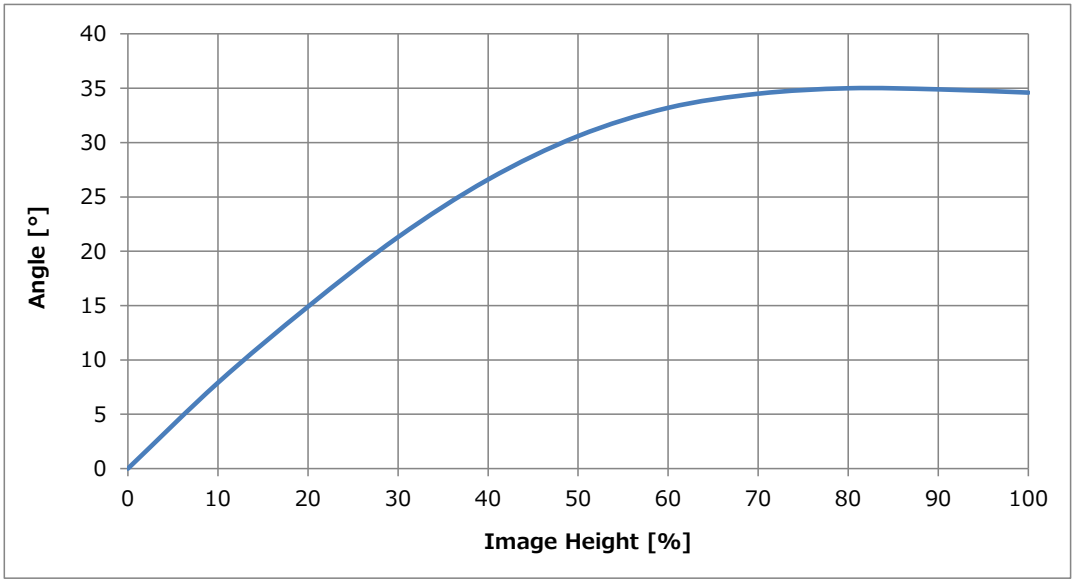


**Figure 32 CRA characteristics**



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## Notes on Handling

### 1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

### 2. Protection from dust and dirt

(1) Perform all work in a clean environment.
(2) Do not touch the chip surface with hand and make any object contact with it.
(3) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

### 3. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Reliability assurance of this product should be ignored because it is a bare chip.
(5) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(6) Note that X-ray inspection may damage characteristics of the sensor.
(7) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.
(8) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.



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## Notes on Handling (Additional items concerning bare chip mounting of stacked-type CMOS image sensors)

Collet contact is allowed in areas other than the pixel area, bonding pads, scribe area, and chip edge. Contact with areas other than the contact-allowed area may result in problems such as dust emission or electrostatic breakdown.

**Collet contact-prohibited areas**

- Pixel area: Abnormal images
- Bonding pad: Circuit electrostatic breakdown
  (Please note that this rule is not applicable for electrostatic breakdown prevention areas.)
- Scribe area: Dust emission due to chipping
- Chip edge: Dust emission due to chip breakage

Note: Ensure sufficient positional accuracy during the pickup work.
Separate the collet contact surfaces and contact-prohibited areas as much as possible.

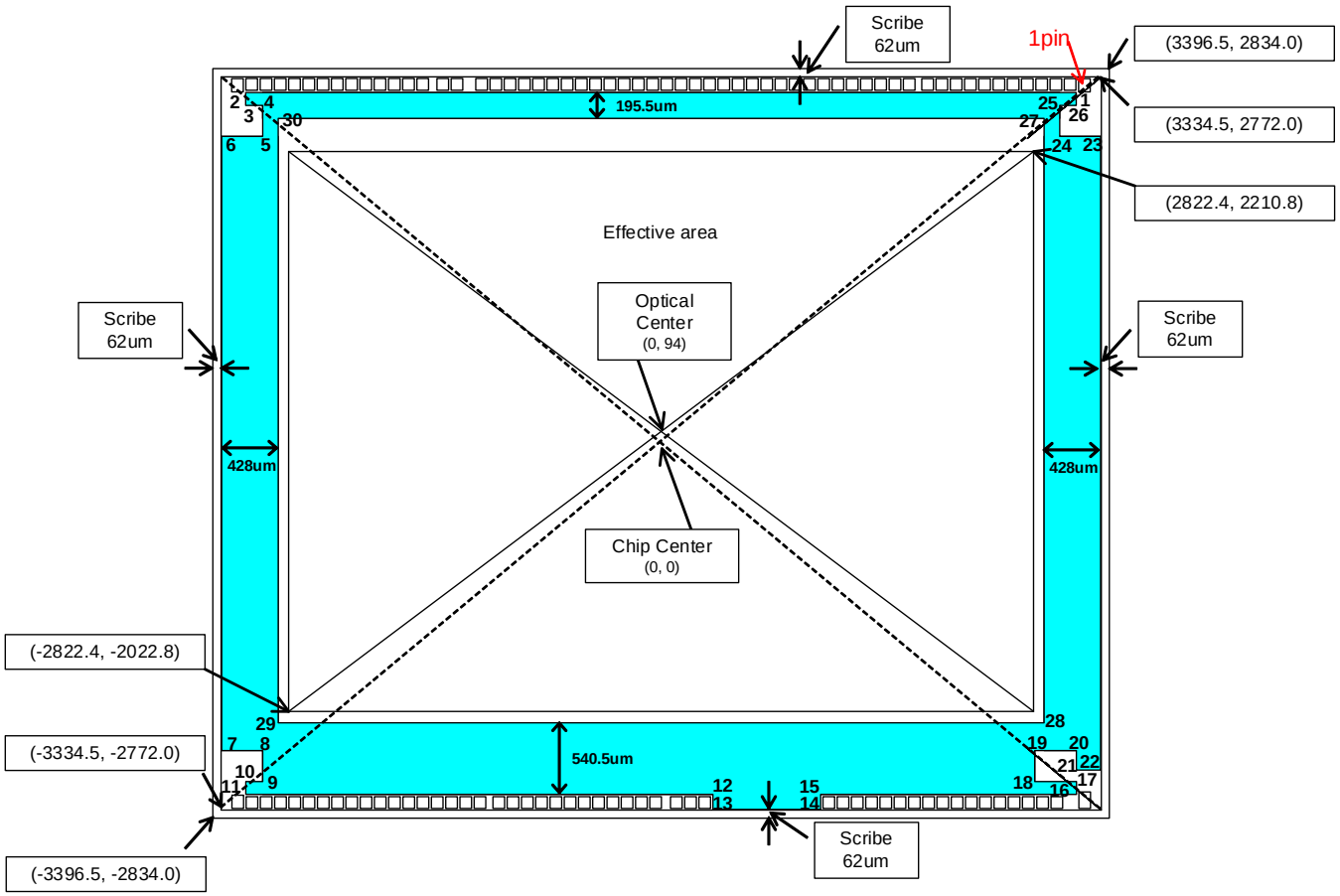


**Figure 33 Contact-allowed area**

Ultrasonic chip cleaning is prohibited.
This may result in dust emission from cut surfaces.

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* $Date:            17. January 2013
* $Revision:        V1.4.1
*
* Project:          CMSIS DSP Library
* Title:            arm_common_tables.h
*
* Description:      This file has extern declaration for common tables like Bitreverse, reciprocal etc which are used across different functions
*
* Target Processor: Cortex-M4/Cortex-M3
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* $Date:            17. January 2013
* $Revision:        V1.4.1
*
* Project:          CMSIS DSP Library
* Title:            arm_const_structs.h
*
* Description:    This file has constant structs that are initialized for
*                   user convenience.    For example, some can be given as
*                   arguments to the arm_cfft_f32() function.
*
* Target Processor: Cortex-M4/Cortex-M3
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* $Revision:        V1.4.1
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* Project:          CMSIS DSP Library
* Title:            arm_math.h
*
* Description:      Public header file for CMSIS DSP Library
*
* Target Processor: Cortex-M4/Cortex-M3/Cortex-M0
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/******************************************************************************//**
  * @file     core_cm0.h
  * @brief    CMSIS Cortex-M0 Core Peripheral Access Layer Header File
  * @version  V3.20
  * @date     25. February 2013
  *
  * @note
  *
  ******************************************************************************/
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/******************************************************************************//**
 * @file     core_cm0plus.h
 * @brief    CMSIS Cortex-M0+ Core Peripheral Access Layer Header File
 * @version  V3.20
 * @date     25. February 2013
 *
 * @note
 *
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/******************************************************************************//**
 * @file     core_cmFunc.h
 * @brief    CMSIS Cortex-M Core Function Access Header File
 * @version  V3.20
 * @date     25. February 2013
 *
 * @note
 *
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/******************************************************************************//**
 * @file     core_cmInstr.h
 * @brief    CMSIS Cortex-M Core Instruction Access Header File
 * @version  V3.20
 * @date     05. March 2013
 *
 * @note
 *
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## Appendix-1 Peripheral Circuit (analog 2.8V only)

The following peripheral circuit shows the case of analog 2.8V only. This mode is available as an option.

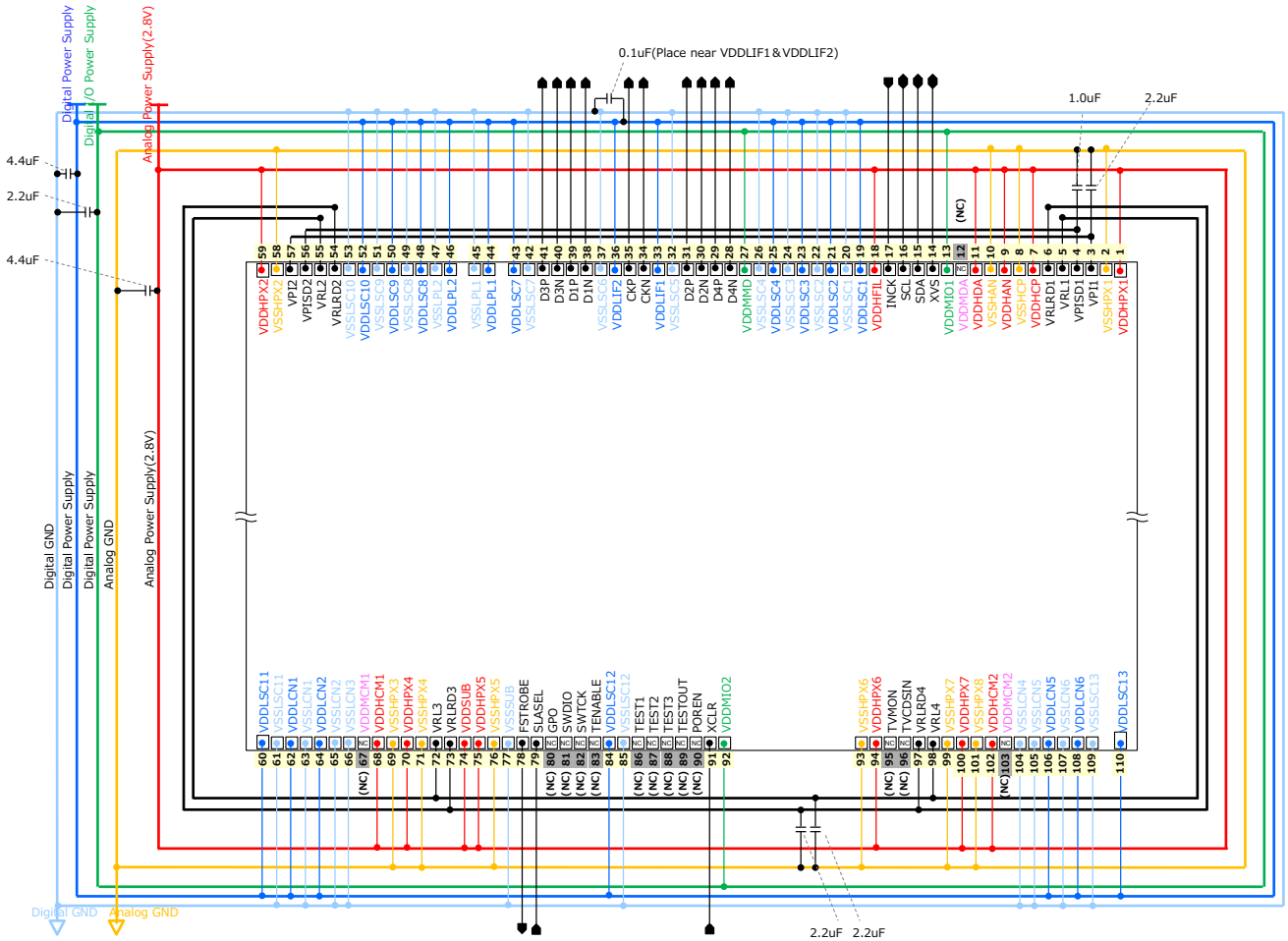


**Figure A-1 Peripheral Circuit (analog 2.8V only)**



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**Table A-1 Pin Description (Analog 2.8V only)**

| No. | Symbol | I/O | A/D | Description | Remarks |
|---|---|---|---|---|---|
| 1 | VDDHPX1 | Power | A | 2.8V Power Supply | |
| 2 | VSSHPX1 | GND | A | 2.8V GND | |
| 3 | VPI1 | Power | A | 2.8V Input | Connect to VPI2 |
| 4 | VPISD1 | Power | A | 2.8V Input | Connect to VPISD2 |
| 5 | VRL1 | Minus | A | -1.2V Input | Connect to VRL2 ,VRL3 and VRL4 |
| 6 | VRLRD1 | Minus | A | -1.2V Input | Connect to VRLRD2 ,VRLRD3 and VRLRD4 |
| 7 | VDDHCP | Power | A | 2.8V Power Supply | |
| 8 | VSSHCP | GND | A | 2.8V GND | |
| 9 | VDDHAN | Power | A | 2.8V Power Supply | |
| 10 | VSSHAN | GND | A | 2.8V GND | |
| 11 | VDDHDA | Power | A | 2.8V Power Supply | 2.8V |
| 12 | VDDMDA | Power | A | 1.8V Power Supply | NC (*) |
| 13 | VDDMIO1 | Power | D | 1.8V Power Supply | |
| 14 | XVS | I/O | D | Digital I/O | |
| 15 | SDA | I/O | D | Digital I/O | I2C pin |
| 16 | SCL | I | D | Digital I/O | I2C pin |
| 17 | INCK | I | D | Digital Input | Clock input |
| 18 | VDDHFIL | Power | A | 2.8V Power Supply | |
| 19 | VDDLSC1 | Power | D | 1.05V Power Supply | |
| 20 | VSSLSC1 | GND | D | 1.05V GND | |
| 21 | VDDLSC2 | Power | D | 1.05V Power Supply | |
| 22 | VSSLSC2 | GND | D | 1.05V GND | |
| 23 | VDDLSC3 | Power | D | 1.05V Power Supply | |
| 24 | VSSLSC3 | GND | D | 1.05V GND | |
| 25 | VDDLSC4 | Power | D | 1.05V Power Supply | |
| 26 | VSSLSC4 | GND | D | 1.05V GND | |
| 27 | VDDMMD | Power | D | 1.8V Power Supply | |
| 28 | D4N | O | D | Digital Output | MIPI output (DATA–) |
| 29 | D4P | O | D | Digital Output | MIPI output (DATA+) |
| 30 | D2N | O | D | Digital Output | MIPI output (DATA–) |
| 31 | D2P | O | D | Digital Output | MIPI output (DATA+) |
| 32 | VSSLSC5 | GND | D | 1.05V GND | |
| 33 | VDDLIF1 | Power | D | 1.05V Power Supply | |
| 34 | CKN | O | D | Digital Output | MIPI output (CLOCK–) |
| 35 | CKP | O | D | Digital Output | MIPI output (CLOCK+) |
| 36 | VDDLIF2 | Power | D | 1.05V Power Supply | |
| 37 | VSSLSC6 | GND | D | 1.05V GND | |
| 38 | D1N | O | D | Digital Output | MIPI output (DATA–) |
| 39 | D1P | O | D | Digital Output | MIPI output (DATA+) |
| 40 | D3N | O | D | Digital Output | MIPI output (DATA–) |



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| No. | Symbol | I/O | A/D | Description | Remarks |
|---|---|---|---|---|---|
| 41 | D3P | O | D | MIPI | MIPI output(DATA+) |
| 42 | VSSLSC7 | GND | D | 1.05V GND | |
| 43 | VDDLSC7 | Power | D | 1.05V Power Supply | |
| 44 | VDDLPL1 | Power | D | 1.05V Power Supply | |
| 45 | VSSLPL1 | GND | D | 1.05V GND | |
| 46 | VDDLPL2 | Power | D | 1.05V Power Supply | |
| 47 | VSSLPL2 | GND | D | 1.05V GND | |
| 48 | VDDLSC8 | Power | D | 1.05V Power Supply | |
| 49 | VSSLSC8 | GND | D | 1.05V GND | |
| 50 | VDDLSC9 | Power | D | 1.05V Power Supply | |
| 51 | VSSLSC9 | GND | D | 1.05V GND | |
| 52 | VDDLSC10 | Power | D | 1.05V Power Supply | |
| 53 | VSSLSC10 | GND | D | 1.05V GND | |
| 54 | VRLRD2 | Minus | A | -1.2V Input | Connect to VRLRD1 ,VRLRD3 and VRLRD4 |
| 55 | VRL2 | Minus | A | -1.2V Input | Connect to VRL1 ,VRL3 and VRL4 |
| 56 | VPISD2 | Power | A | 2.8V Input | Connect to VPISD1 |
| 57 | VPI2 | Power | A | 2.8V Input | Connect to VPI1 |
| 58 | VSSHPX2 | GND | A | 2.8V GND | |
| 59 | VDDHPX2 | Power | A | 2.8V Power Supply | |
| 60 | VDDLSC11 | Power | D | 1.05V Power Supply | |
| 61 | VSSLSC11 | GND | D | 1.05V GND | |
| 62 | VDDLCN1 | Power | D | 1.05V Power Supply | |
| 63 | VSSLCN1 | GND | D | 1.05V GND | |
| 64 | VDDLCN2 | Power | D | 1.05V Power Supply | |
| 65 | VSSLCN2 | GND | D | 1.05V GND | |
| 66 | VSSLCN3 | GND | D | 1.05V GND | |
| 67 | VDDMCM1 | Power | A | 1.8V Power Supply | NC (*) |
| 68 | VDDHCM1 | Power | A | 2.8V Power Supply | 2.8V |
| 69 | VSSHPX3 | GND | A | 2.8V GND | |
| 70 | VDDHPX4 | Power | A | 2.8V Power Supply | |
| 71 | VSSHPX4 | GND | A | 2.8V GND | |
| 72 | VRL3 | Minus | A | -1.2V Input | Connect to VRL1 ,VRL2 and VRL4 |
| 73 | VRLRD3 | Minus | A | -1.2V Input | Connect to VRLRD1 ,VRLRD2 and VRLRD4 |
| 74 | VDDSUB | Power | A | 2.8V Power Supply | |
| 75 | VDDHPX5 | Power | A | 2.8V Power Supply | |
| 76 | VSSHPX5 | GND | A | 2.8V GND | |
| 77 | VSSSUB | GND | D | 1.05V GND | |
| 78 | FSTROBE | O | D | Digital Output | Flash strobe |
| 79 | SLASEL | I | D | Digital Input | Slave address control<br>(pull-down) |
| 80 | GPO | O | D | Digital Output | NC |



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| No. | Symbol | I/O | A/D | Description | Remarks |
|---|---|---|---|---|---|
| 81 | SWDIO | I/O | D | Digital I/O | NC |
| 82 | SWTCK | I | D | Digital Input | NC |
| 83 | TENABLE | I | D | Digital Input | NC(pull-down) |
| 84 | VDDLSC12 | Power | D | 1.05V Power Supply | |
| 85 | VSSLSC12 | GND | D | 1.05V GND | |
| 86 | TEST1 | I | D | Digital Input | NC |
| 87 | TEST2 | I | D | Digital Input | NC |
| 88 | TEST3 | I | D | Digital Input | NC |
| 89 | TESTOUT | O | D | Digital Output | NC |
| 90 | POREN | I | D | Digital Input | NC |
| 91 | XCLR | I | D | Digital Input | |
| 92 | VDDMIO2 | Power | D | 1.8V Power Supply | |
| 93 | VSSHPX6 | GND | A | 2.8V GND | |
| 94 | VDDHPX6 | Power | A | 2.8V Power Supply | |
| 95 | TVMON | O | A | Analog Output | NC |
| 96 | TVCDSIN | I | A | Analog Input | NC |
| 97 | VRLRD4 | Minus | A | -1.2V Input | Connect to VRLRD1 ,VRLRD2 and VRLRD3 |
| 98 | VRL4 | Minus | A | -1.2V Input | Connect to VRL1 ,VRL2 and VRL3 |
| 99 | VSSHPX7 | GND | A | 2.8V GND | |
| 100 | VDDHPX7 | Power | A | 2.8V Power Supply | |
| 101 | VSSHPX8 | GND | A | 2.8V GND | |
| 102 | VDDHCM2 | Power | A | 2.8V Power Supply | 2.8V |
| 103 | VDDMCM2 | Power | A | 1.8V Power Supply | NC (*) |
| 104 | VSSLCN4 | GND | D | 1.05V GND | |
| 105 | VSSLCN5 | GND | D | 1.05V GND | |
| 106 | VDDLCN5 | Power | D | 1.05V Power Supply | |
| 107 | VSSLCN6 | GND | D | 1.05V GND | |
| 108 | VDDLCN6 | Power | D | 1.05V Power Supply | |
| 109 | VSSLSC13 | GND | D | 1.05V GND | |
| 110 | VDDLSC13 | Power | D | 1.05V Power Supply | |

Note : The pin shall be "NC(No Connection)" in this case(VANA1=VANA2=2.8V).



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**Table A-2 DC Characteristics (Analog 2.8V only)**

| Item | Pins | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Supply voltage | VDDHPX1,2,4,5,6,7 | VANA1 | 2.8V supply | 2.7 | 2.8 | 2.9 | V |
| | VDDHCM1,2 | | | | | | |
| | VDDHAN | | | | | | |
| | VDDHDA | | | | | | |
| | VDDHFIL | | | | | | |
| | VDDSUB | | | | | | |
| | VDDHDA | VANA2 | 2.8V supply | 2.7 | 2.8 | 2.9 | |
| | VDDHCM1,2 | | | | | | |
| | VDDMDA | | (*) | N.C. | N.C. | N.C. | |
| | VDDMCM1,2 | | | | | | |
| | VDDMIO1,2, VDDMMD | VIF | | 1.7 | 1.8 | 1.9 | V |
| | VDDLCN1,2,5,6 | VDIG | | 0.95 | 1.05 | 1.15 | V |
| | VDDLSC1,2,3,4,7,8, 10,11,12,13 | | | | | | |
| | VDDLIF1,2 | | | | | | |
| | VDDLPL1,2 | | | | | | |
| Digital input voltage | SDA, SCL | VIH | | 0.7VIF | | 2.9 | V |
| | | VIL | | -0.3 | | 0.3VIF | V |
| Digital input voltage | XCLR, INCK SLASEL XVS | VIH | | 0.65VIF | | VIF + 0.3 | V |
| | | VIL | | -0.3 | | 0.35VIF | V |
| Digital output voltage | SDA, FSTROBE XVS | VOH | | VIF-0.4 | | | V |
| | | VOL | | | | 0.4 | V |

Note : The pin shall be "NC(No Connection)" in this case(VANA1=VANA2=2.8V).



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